Analysis of Temporal Noise in CMOS APS

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ABSTRACT

Temporal noise sets a fundamental limit on image sensor performance, especially under low illumination and in video applications. In a CCD image sensor, temporal noise is well studied and characterized. It is primarily due to the photodetector shot noise and the thermal and 1/f noise of the output charge to voltage amplifier. In a CMOS APS several additional sources contribute to temporal noise, including the noise due to the pixel reset, follower, and access transistors. The analysis of noise is further complicated by the nonlinearity of the APS charge to voltage characteristics, which is becoming more pronounced as CMOS technology scales, and the fact that the reset transistor operates below threshold for most of the reset time. The paper presents an accurate analysis of temporal noise in APS. We analyze the noise for each stage of the sensor operation, and identify the noise contribution from each source. We analyze noise due to photodetector shot noise taking nonlinearity into consideration. We find that nonlinearity improves SNR at high illumination. Using an MOS transistor subthreshold noise model we show that the noise due to the reset transistor shot noise is at most half the commonly quoted $\frac{kT}{C}$ (V^2) value. Using HSPICE simulation, we find the noise due to the follower and access transistors. As expected we find that at low illumination reset noise dominates, while at high illumination photodetector shot noise dominates. Finally, we present experimental results from test structures fabricated in 0.35μ CMOS processes. We find that both measured peak SNR and reset noise values match well with the results of our analysis.

Keywords: temporal noise, subthreshold operation, reset noise, shot noise, CMOS APS, image sensor

1. INTRODUCTION

Temporal noise sets a fundamental limit on image sensor performance, especially under low illumination and in video applications. In a CCD image sensor, temporal noise is well studied and characterized.[1] It is primarily due to the photodetector shot noise and the thermal and 1/f noise of the output charge to voltage amplifier. In a CMOS APS several additional sources contribute to temporal noise. These include the thermal, shot, and 1/f noise of the pixel reset, follower, and access transistors. Hand analysis of temporal noise in APS has been published by several authors.[2,3] Their analysis shows that at low illumination the largest noise component is due to the reset transistor noise, and that at high illumination the largest noise component is due to the photodetector shot noise. Their estimates of these two noise components, however, are inaccurate. In analyzing the reset transistor noise they assume steady state conditions and conclude that the mean square value of the noise sampled at the end of the reset is simply $\frac{kT}{C}$ (V^2). In practice reset time is not long enough to achieve steady state. In estimating the shot noise component they ignore the nonlinearity of the photodetector charge to voltage characteristics. This nonlinearity is becoming more pronounced as supply voltage scales with technology, and can no longer be ignored.

In this paper we present an accurate analysis of noise in APS. Using the MOS transistor subthreshold shot noise model[4] we show that the noise due to the reset transistor shot noise is at most half the commonly quoted $\frac{kT}{C}$ (V^2) value. We analyze the noise due to the photodetector shot noise taking nonlinearity into consideration. We find that nonlinearity improves SNR at high illumination. Using HSPICE simulation, we find the noise contributions of the follower and access transistor thermal and 1/f noise. As expected we find that at low illumination reset noise dominates, while at high illumination photodetector shot noise dominates. Finally, we present experimental results from test structures fabricated in 0.35μ CMOS processes. We find

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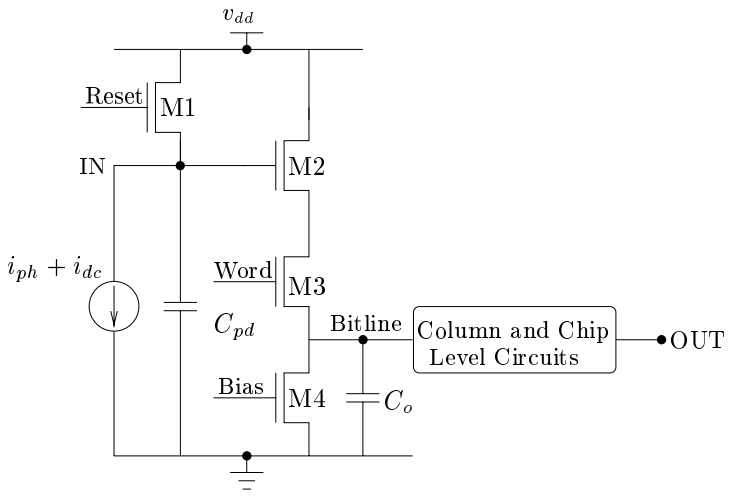

Figure 1. APS circuit.

that both measured peak SNR and reset noise values match well with the results of our hand analysis and simulations.

The APS circuit we analyze in this paper is the standard photodiode, three transistors per pixel circuit shown in Figure 1. The capacitor C_{pd} shown in the figure represents the equivalent photodiode capacitance. To complete the signal path we also show the column bias transistor and storage capacitor C_o. We are interested in finding the input referred RMS noise value at IN in volts.

To find the RMS input referred noise voltage, we consider the noise generated during each stage of the APS operation, i.e., during reset, integration, and readout. We do not analyze the effect of the 1/f noise due to the photodetector and reset transistor, since it is much smaller than the shot noise effect. We do not consider the effect of CDS on noise in this paper*. We also ignore the fact that the stored noise voltage decays during integration and before it is sampled.[3] The noise generated during reset and integration are sampled onto C_o, and then transferred to the output during readout.

The remainder of this paper is organized as follows. In section 2 we analyze noise during integration. In section 3 we analyze noise during reset due to shot noise. In section 4 we provide both hand analysis and HSPICE simulation results for noise during readout due to the follower and access transistors thermal and 1/f noise. Finally, in section 5 we present experimental results that corroborate our analysis results.

2. NOISE DURING INTEGRATION

During integration, the dominant noise source is shot noise $I_s(t)$ due to the dark current i_{dc} and the photocurrent i_{ph}, which is well modelled as white gaussian noise with two sided power spectral density (psd)

$$S_{I_s}(f) = q(i_{ph} + i_{dc}) \text{ A}^2/\text{Hz}. \tag{1}$$

To analyze noise we let $V_{pd}(t) = v_{pd}(t) + V_n(t)$ be the voltage on the photodiode during integration, where $v_{pd}(t)$ is the signal voltage, and $V_n(t)$ is the noise voltage. It then follows that

$$\frac{dV_{pd}(t)}{dt} = -\frac{i_{ph} + i_{dc} + I_s(t)}{C_{pd}(V_{pd}(t))}. \tag{2}$$

If the photodiode capacitance is constant over the integration time, it is easy to show that the mean square value of the noise voltage sampled at the end of integration, i.e., at t_{int}, is given by

$$\overline{V_n^2(t_{int})} = \frac{q(i_{ph} + i_{dc})}{C_{pd}^2} t_{int}. \tag{3}$$

*CDS increases the reset noise component due to shot noise but reduces the 1/f noise component.

The photodiode capacitance, however, is a function of its reverse bias voltage. As a result the photodiode output voltage is nonlinear in its input current. Assuming that the noise is much smaller than the signal, we can write the noise part of equation 2 by

$$\frac{dV_n(t)}{dt} - \frac{1}{C_{pd}^2(v_{pd}(t))}\frac{dC_{pd}(v_{pd}(t))}{dv_{pd}(t)}V_n(t)(i_{ph}+i_{dc}) = -\frac{I_s(t)}{C_{pd}(v_{pd}(t))}. \tag{4}$$

The mean square value of V_n at the end of integration is thus given by

$$\overline{V_n^2(t_{int})} = q(i_{ph}+i_{dc})\int_0^{t_{int}} \frac{1}{C_{pd}^2(v_{pd}(\tau))} e^{-2(i_{ph}+i_{dc})\int_\tau^{t_{int}} \frac{d(1/C_{pd}(v_{pd}(\tau_0)))}{dv_{pd}(\tau_0)}d\tau_0} d\tau. \tag{5}$$

Note that equation 3 follows from this more general equation if we assume that C_{pd} is constant during integration. To take the dependency of the photodiode capacitance on the reverse bias voltage into consideration, we make the simplifying assumption of an abrupt pn to get that

$$C_{pd}(v_{pd}(t)) = C_{pd}(v_{pd}(0))\sqrt{\frac{v_{pd}(0)+\phi}{v_{pd}(t)+\phi}}, \tag{6}$$

where ϕ is the built in junction potential, and $v_{pd}(0)$ is the voltage on C_{pd} at the beginning of integration. Solving the deterministic part of equation 2 we find that

$$v_{pd}(t) = v_{pd}(0) - \frac{(i_{ph}+i_{dc})}{C_{pd}(v_{pd}(0))}t + \frac{(i_{ph}+i_{dc})^2 t^2}{4C_{pd}^2(v_{pd}(0))(v_{pd}(0)+\phi)}. \tag{7}$$

We can now explicitly express $C_{pd}(v_{pd}(t))$ as a function of t. Substituting into equation 5, we get that

$$\overline{V_n^2(t_{int})} = \frac{q(i_{ph}+i_{dc})}{C_{pd}^2(v_{pd}(0))}t_{int}(1 - \frac{1}{2(v_{pd}(0)+\phi)}\frac{i_{ph}+i_{dc}}{C_{pd}(v_{pd}(0))}t_{int})^2. \tag{8}$$

To demonstrate the effect of varying capacitance during integration, we consider an example with $v_{pd}(0)$=2.1V, $C_{pd}(v_{pd}(0)) = 22fF$, i_{dc}=2.28fA, $\phi = 0.7$V, and $t_{int} = 30$ms. These numbers were picked to be consistent with the parameters of the test structures used in the measurements presented in section 5. Figure 2 plots the signal $v_{pd}(t_{int})$ and the input referred RMS value of the noise as a function of the photocurrent i_{ph} for both constant and varying C_{pd}. Note that the effect of nonlinearity is only pronounced for large signal values, and results in reductions in both the signal and the noise. The signal to noise ratio, however, improves as we shall see later.

3. NOISE DURING RESET

During reset M3 is turned off and a v_{dd} pulse is applied to the gate of M1. At the beginning, and for a very short amount of time, M1 is in the saturation region. It then goes below threshold for the rest of the reset time. In the subthreshold region the transistor noise is mainly due to shot noise with two sided psd given by[4]

$$S_{I_d}(f) = qi_d \text{ A}^2/\text{Hz}, \tag{9}$$

where i_d is the drain current of M1. If the reset time t_r is greater than the settling time t_{settle}, i.e., the time at which the transistor subthreshold current equals the photodiode current $i_{ph}+i_{dc}$, then the average reset noise power is given by[5]

$$\overline{V_n^2} = \int_{-\infty}^{\infty} \frac{2q(i_{ph}+i_{dc})}{(g_{m1}+g_{mb1})^2}\frac{1}{1+(2\pi f\frac{C_{pd}}{(g_{m1}+g_{mb1})})^2}df, \tag{10}$$

where g_{m1} and g_{mb1} are the transconductances of M1 in subthreshold, and the factor of 2 is due to the fact that in steady state $i_d = i_{ph}+i_{dc}$. Performing the integral we get that

$$\overline{V_n^2} = \frac{q(i_{ph}+i_{dc})}{C_{pd}(g_{m1}+g_{mb1})}. \tag{11}$$

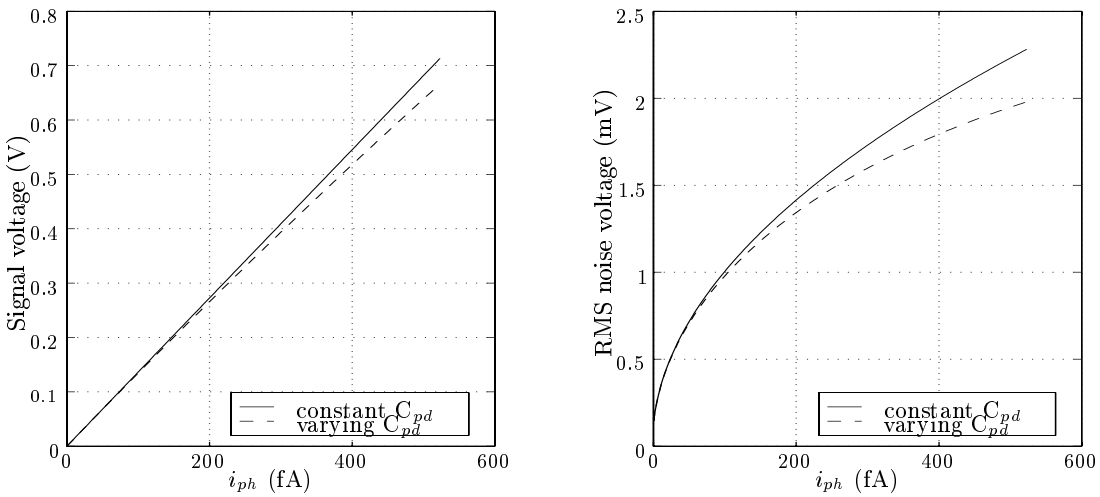

Figure 2. Signal and noise levels as functions of input photocurrent.

Since in subthreshold $i_d = \frac{kT}{q}(g_{m1} + g_{mb1})$, $\overline{V_n^2} = \frac{kT}{C_{pd}}$, which is consistent with the often quoted value.[2,3,5,6]

This analysis, however, is valid only if steady state is achieved during reset [†]. To find out if steady state is achieved during reset we compute the settling time t_{settle}, which is simply done by solving the differential equation

$$\frac{dv_{pd}(t)}{dt} = -\frac{i_{ph} + i_{dc}}{C_{pd}(v_{pd}(t))} + \frac{i_d(t)}{C_{pd}(v_{pd}(t))}. \tag{12}$$

When M1 operates above threshold

$$i_d(t) = \frac{W}{2L} C_{ox} \mu_n (v_{dd} - v_{th}(v_{pd}) - v_{pd})^2, \tag{13}$$

where the threshold voltage

$$v_{th}(v_{pd}) = 0.75 + 0.65(\sqrt{v_{pd} + 0.7} - \sqrt{0.7}) \quad \text{V}. \tag{14}$$

For most of the reset time M1 operates in subthreshold, and i_d can be expressed as[7]

$$i_d(t) = \frac{W}{L} I_0 e^{\left[\frac{(v_g - v_{pd})\kappa}{v_T} - \frac{(v_{pd} - v_b)(1-\kappa)}{v_T}\right]} (1 - e^{\frac{(v_d - v_{pd})}{v_T}}), \tag{15}$$

where v_g is the gate voltage, v_d is the drain voltage, v_{pd} is the source voltage, v_b is the bulk voltage, κ is the gate efficiency factor, $v_T = \frac{kT}{q}$, and I_0 is a constant that depends on the transistor threshold voltage. The transition between above and below threshold is somewhat arbitrary. We assume that it occurs when the currents calculated by equations 13 and 15 are equal. Solving equation 12 assuming above and below threshold operation, we find that the transition is $\approx$2V, which is achieved after $t_1 \leq 0.2$ns (depending on the voltage $v_{pd}(0)$ at the beginning of the reset). We find that the settling time $t_{settle} \geq 1$ms even for very high photocurrents. Reset times are typically in the range of few microseconds and thus the circuit is not operating in steady state and we must analyze the reset noise under non-steady state conditions.

To find the reset noise under non-steady state condition, we consider the small signal circuit equation with time varying parameters

$$I_n(t) = C_{pd}(t)\frac{dV_n(t)}{dt} + g(t)V_n(t), \tag{16}$$

[†]Under very low illumination, M1 may be in the subthreshold region from the beginning of the reset. The analysis of this case can be done using the same method we describe here. In video applications a low illumination may persist for many frames. In this case steady state may be approached, and the noise increases accordingly until it reaches its maximum value of $\frac{kT}{C_{pd}}$.

where $I_n(t)$ is the noise source current, $V_n(t)$ is the reset noise voltage, and $g(t)$ is the total transistor transconductance. Solving this equation we find that at the end of reset, i.e., at t_r, the mean square noise voltage

$$\overline{V_n^2(t_r)} = \int_0^{t_r} \frac{N(\tau)}{C_{pd}^2(\tau)} e^{-2\int_\tau^{t_r} \frac{g(\tau_0)}{C_{pd}(\tau_0)} d\tau_0} d\tau, \tag{17}$$

where $N(\tau)$ is the psd of the (white) noise source. It can be readily verified from equation 17 that the contribution from the noise above threshold is extremely small, and can thus be ignored. We also ignore the noise associated with $i_{ph} + i_{dc}$, since it is much smaller than the subthreshold current. With these simplifying assumptions, $N(\tau) = q i_d(\tau)$, and $C_{pd}(\tau)$ is a constant, which we denote by C_{pd}. Solving equation 12 using equation 15, we find that

$$i_d(\tau) = \frac{v_T C_{pd}}{\tau - t_1 + \delta}, \tag{18}$$

where $\delta = \frac{v_T C_{pd}}{i_d(t_1)}$. Carrying out the integral of equation 17, we find that

$$\overline{V_n^2(t_r)} = \frac{1}{2}\frac{kT}{C_{pd}}(1 - \frac{\delta^2}{(t_r - t_1 + \delta)^2}). \tag{19}$$

Thus the mean square reset noise voltage is less than $\frac{1}{2}$ of the often quoted $\frac{kT}{C_{pd}}$ value. Since t_r is typically much larger than t_1 and δ, the mean square reset noise voltage value is in fact very close to $\frac{1}{2}\frac{kT}{C_{pd}}$. Using values of $C_{pd} = 22$fF and $T = 293$K, we get an input referred RMS reset noise voltage of 303μV.

4. NOISE DURING READOUT

During readout, noise is due to transistors M2, M3, M4, and the column and chip level circuits thermal and 1/f noise. Ignoring the noise contributions of the column and chip level circuits, which are very small, and the 1/f noise, readout noise can be easily computed via the small signal circuit in Figure 3. In this figure, $I_{M2}(t)$, $V_{M3}(t)$, and $I_{M4}(t)$ are the thermal noise sources associated with M2, M3, and M4, respectively, g_{m2} and g_{m4} are the transconductances of M2 and M4, g_{d3} is the channel conductance of M3, and C_o is the column storage capacitance including the bitline capacitance. Assuming steady state, which is well justified here, it can be easily shown that the bitline referred mean square noise voltages due to M2, M3, and M4 are given by

$$\overline{V_{n,M2}^2} = \frac{2}{3}\frac{kT}{C_o}\frac{1}{1 + \frac{g_{m2}}{g_{d3}}}, \tag{20}$$

$$\overline{V_{n,M3}^2} = \frac{kT}{C_o}\frac{1}{g_{d3}(\frac{1}{g_{d3}} + \frac{1}{g_{m2}})}, \text{and} \tag{21}$$

$$\overline{V_{n,M4}^2} = \frac{2}{3}\frac{kT}{C_o} g_{m4}(\frac{1}{g_{d3}} + \frac{1}{g_{m2}}), \tag{22}$$

repectively.

To obtain more accurate results for noise during readout (including 1/f noise), we use HSPICE. We sweep the IN voltage, perform DC analysis to determine the circuit bias point for each IN voltage value, and then perform AC noise analysis. Using this methodology, we simulated our APS circuit including the column and chip level circuits.[8] As expected, the noise contributions from column and chip level circuits were found to be very small. To compare the contributions of M2, M3, and M4 during readout we plot the simulated output referred psd for each in Figure 4. Note that except when the IN voltage is near its reset value, the noise from M3 is several orders of magnitude lower than the noise from M2 and M4. Summing up the contributions from the three transistors to the total output noise, we find that the output referred RMS noise voltage from the readout stage to be around 63μV, independent of the IN voltage value. Using the simulated IN to OUT voltage gain value of 0.81, this is equivalent to an input referred value of 78μV.

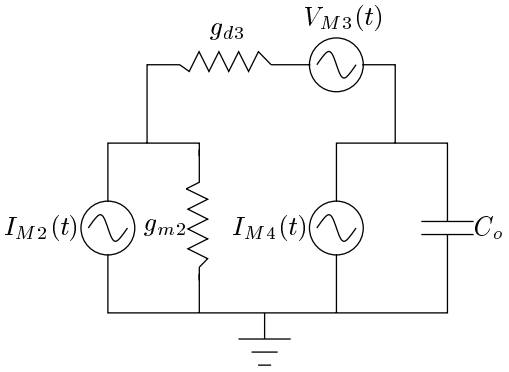

Figure 3. Small signal model for noise analysis during readout.

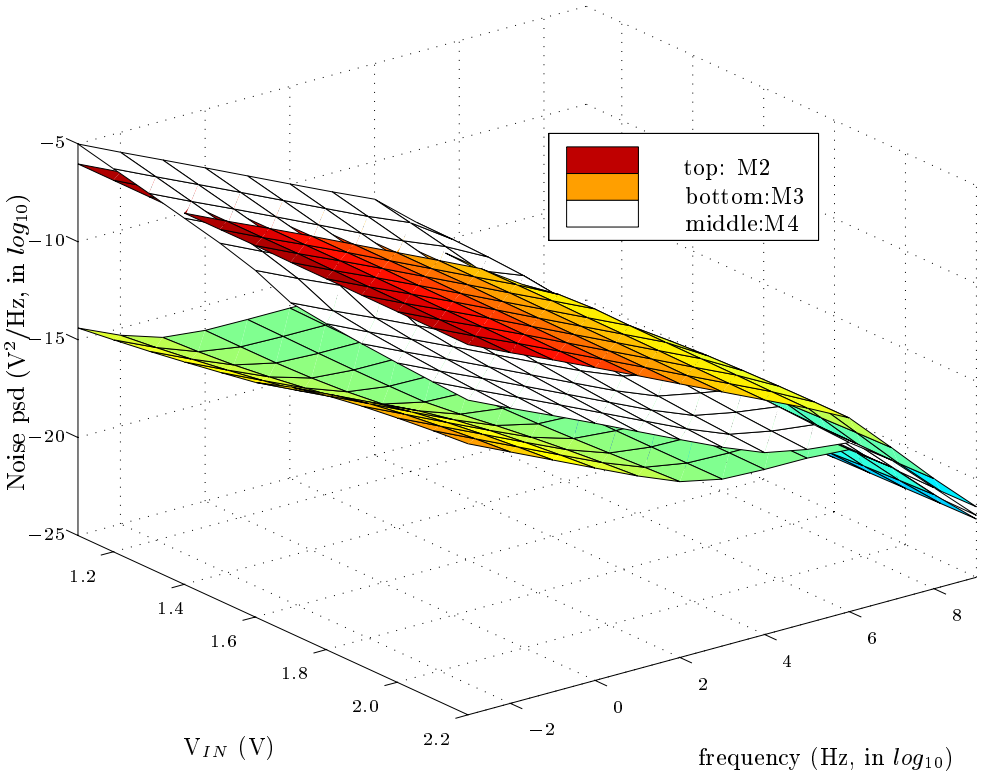

Figure 4. Readout noise psd due to M2, M3, and M4.

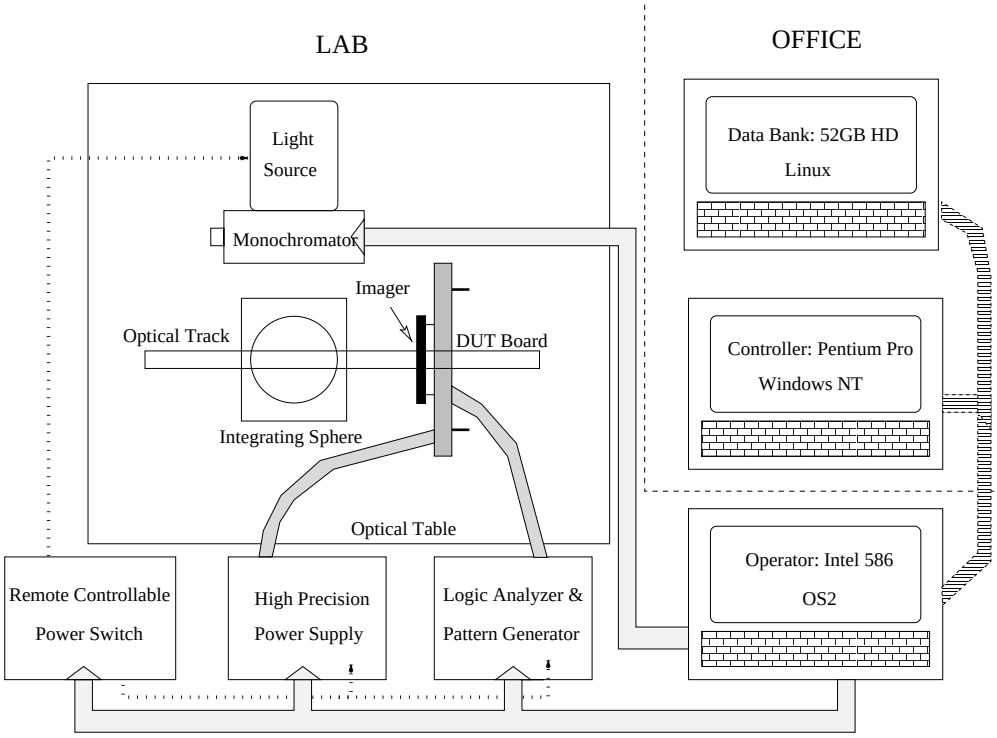

Figure 5. Experimental Setup

5. EXPERIMENTAL RESULTS

In this section, we present noise measurement results from our 64×64 pixel APS test structure,[8] which were fabricated in a 0.35μ standard digital CMOS process. We compare the measured results to the analysis results presented in the previous sections. The comparison is well justified since the circuit parameter values assumed in the analysis were extracted from the test structure circuit. The optical and electrical setup are basically the same as the one we used to measure QE[9] and FPN.[10] The analog output from our sensor is first amplified using an LNA, then digitized using a 16-bit ADC.

To measure noise special care must be taken to reduce environmental interference, which can be caused by many sources including light source fluctuations, temperature fluctuations, and electromagnetic interference. To do so, we housed the setup in a well air conditioned dark room. We used a light source with intensity fluctuations of less than 0.5%. Temperature and light intensity were recorded each time data was taken. We repeated the measurements many times so that any remaining environmental interference can be averaged out. The measurements were taken remotely using the setup depicted in Figure 5.

In taking the noise measurements we first determined the board level noise, including the LNA noise and ADC quantization noise. This was done by directly driving OUT with a low noise DC voltage source. The measured output referred RMS noise voltage was found to be 82 μV, which is comparable to the estimated readout stage noise, but much lower than the reset noise. As a result reset noise can still be accurately measured. To measure the reset noise we reset the pixel and immediately read the output voltage. This is repeated many times for several different reset times, from 1 μs to 10 μs, at several illumination levels. The measured RMS noise voltage was around 285μV independent of illumination and of reset time. The analysis results by comparison yielded 253μV due to the reset and readout noise, which is quite close given that we ignored the 1/f noise in our analysis of the reset noise.

We also measured the overall RMS noise voltage under different illumination levels[‡]. In Figure 6 we plot the measured and the calculated signal to noise ratios (SNR) versus the output signal. Two calculated SNR

[‡]Actually we measured it under the same illumination, but at varying integration times as discussed in.[9]

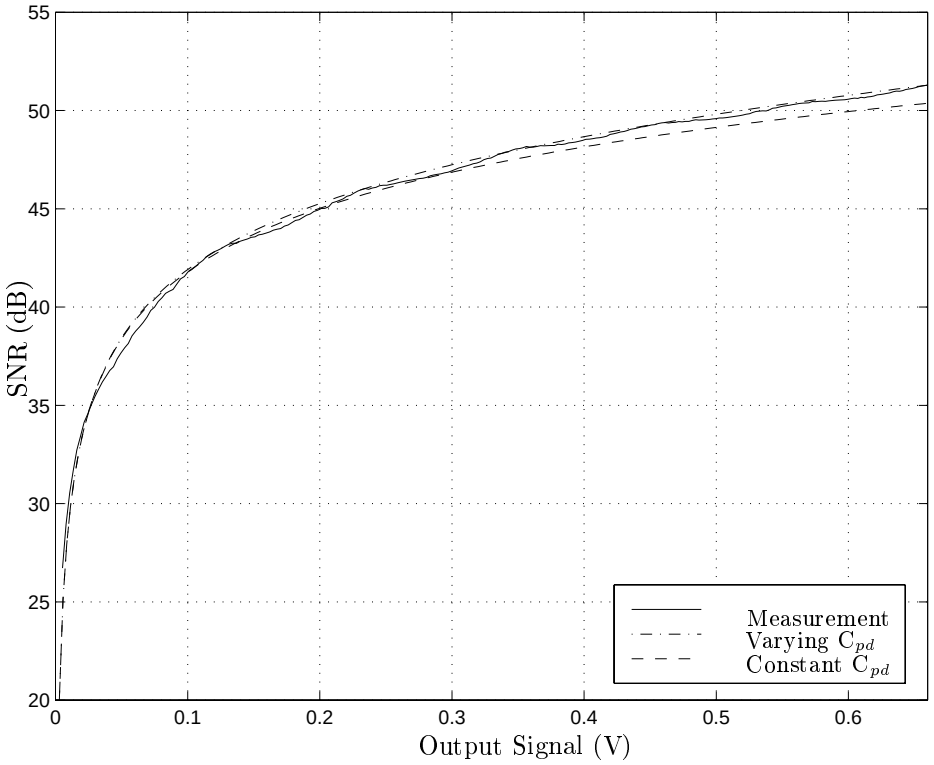

Figure 6. Simulated vs. measured SNR.

curves are given, one assuming constant photodiode capacitance, and the other assuming varying photodiode capacitance as discussed in section 2. Note that the measured SNR curve is very close to the calculated curve assuming varying capacitance, but that the curve assuming constant capacitance becomes slightly lower than the others at high illumination levels.

6. CONCLUSION

We provided an accurate analysis of noise in CMOS photodiode APS. We analyzed noise due to the photodetector shot noise taking nonlinearity into consideration and found that nonlinearity improves SNR at high illumination. We used the MOS transistor subthreshold noise model to analyze reset noise. We found that reset noise is very close to half the commonly quoted $\frac{KT}{C}$ value due to the fact that the reset time is not long enough for the circuit to be in steady state. In deriving this result we assumed that reset is performed by driving the reset transistor gate to v_{dd}. To obtain larger signal swing, i.e., well capacity, or to eliminate image lag the reset transistor gate is sometimes pumped up to $v_{dd} + v_{th}$, or a PMOS transistor is used instead. In these cases, the reset noise value becomes $\frac{KT}{C}$, i.e., increasing signal swing doubles the mean square value of the noise! Finally, we presented experimental results obtained from test structures that were fabricated in 0.35μ CMOS processes, which corroborate the results from our analysis.

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