18.1 A W-Band Transceiver Array with 2.4GHz LO Synchronization Enabling Full Scalability for FMCW Radar

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Closing the angular resolution gap between CMOS radar and optical imaging systems can enable an entirely new cost-effective radar-centric perception solution, but requires extremely large transceiver (TRX) arrays to achieve LiDAR-like angular resolution. Multi-chip cascading of mm-wave radars [1-3] has become the norm to enable these large TRX arrays, but the size of these arrays is still limited due to challenges in achieving low-cost signal distribution across a large aperture. Today, multi-chip radar cascading solutions use mm-wave LO frequencies (20GHz [1,2], 40GHz [3]) along with on-chip frequency multipliers with modest multiplication factors (×4 [1,2], ×2 [3]). However, operating at these frequencies is cost-prohibitive and severely limits the size of the array [1]. For example, for a 64-TX and 64-RX array, the calculated path loss on a Rogers 3003 substrate in an H-tree distribution network reaches 87dB at 40GHz, which requires more than 70 amplifiers with 15dBm output power and 25dB gain alongside the distribution network to compensate the loss. Moreover, maintaining phase coherency required for FMCW systems is also infeasible for such amplifier implementations. Thus, enabling truly scalable TRX arrays requires signal distribution at much lower LO frequencies, which introduces fundamental performance challenges.

In this work, we propose a fully scalable radar TRX architecture with an on-chip ×35 frequency multiplier to enable 2.4GHz LO synchronization while overcoming unique challenges posed by using multiplication factors an order of magnitude higher than previously demonstrated [1-3]. The conceptual MIMO array is shown in Fig. 18.1.1, where multiple 4-channel RX chips form a dense array with antennas spaced by half the wavelength, and multiple 1-channel TX chips form a sparse array. The LO distribution network is formed by on-board transmission lines and commercial power-divider MMIC. An external 2.4GHz FMCW chirp feeds the board as the common reference. In the RX chip, the distributed 2.4GHz chirp goes into an LO generation circuit, where the 2.4GHz signal is multiplied by 35. Then, the generated signal is split into four, goes into an I/Q Hybrid, and drives an N-path mixer-first RX [4]. An IF amplifier finally amplifies the downconverted signal. In the TX chip, the same LO generation circuit multiplies the input signal by 35. A quadrature mixer, which can act as a phase-shifter, a variable gain amplifier, a modulator, or an RF switch to increase the system functionality, processes the LO signal and drives a PA.

A key element of the TRX architecture is the ×35 frequency multiplier. Although frequency multipliers have been widely used in radars [1-3], a high-factor frequency multiplier results in fundamentally new challenges related to the phase noise (PN) and harmonic rejection ratio (HRR) for wideband FMCW radar systems, as shown in Fig. 18.1.2. As a coherent system, the PN from the common reference is removed after de-chirping, while the PN from the frequency multiplier, which is uncorrelated, adds to IF noise floor and decreases the system SNR. Therefore, an extremely low-PN frequency multiplier is needed. A PLL is thus unsuitable due to its high noise property. On the other hand, undesired harmonic spurs generated by frequency multipliers become spurs in IF [5] and limit the system's SFDR. This problem becomes even worse in a high-factor frequency multiplier because the closest harmonic falls in-band of RF channels and cannot be removed by filtering. As a result, we cannot simply cascade frequency multipliers for a higher multiplication factor. From a system perspective, the achievable SFDR is equal to twice the HRR in dB scale, which means a 50dBc HRR is required for a 100dB SFDR. To alleviate the PN and harmonic rejection challenges, in this work, we propose an injection-locked frequency-multiplier (ILFM)-based high-factor frequency multiplication with enhanced harmonic rejection.

The LO generation is achieved by cascading a ×7 low-frequency ILFM (LF-ILFM) and a ×5 high-frequency ILFM (HF-ILFM) as shown in Fig. 18.1.2. A single-ended sinusoidal signal feeds into a pulse generator (PG) and generates harmonic-rich differential pulses, which contain the desired 7th harmonic. The pulses flow into an LF-ILFM and lock the ILFM at the 7th harmonic frequency. Circuit schematics for LO generation are shown in Fig. 18.1.3. Since the LF-ILFM will be followed by a ×5 HF-ILFM, a 14dB (20logN) HRR degradation appears, which means a 64dB HRR is required for a 100dB SFDR. Note that the undesired harmonics from LF-ILFM are spaced by 2.4GHz from the center frequency, and they will be inside the RF band after HF-ILFM. Therefore, the harmonics must be suppressed before the HF-ILFM. We adopt two mechanisms to improve the HRR: a duty-cycle correction (DCC) circuit and an injection-locked buffer (IL-BUF).

First, the DCC circuit adjusts the pulse position after the PG. Because the PG generates differential pulses, any mismatch in the pulse position may lead to the increase of even harmonics, which are the closest harmonics (6th and 8th harmonics) to the desired 7th harmonic. By sensing the pulse position through an AND gate and converting it to a differential square wave by a D-latch, the pulse-position information is within the duty-cycle of the square wave and can be captured by observing its DC value by a lowpass filter. The error signal is then used to control the bias of the input buffer to set the threshold of the inverter and adjust the duty-cycle of the square wave after the input buffer. Thus, the pulse position is adjusted accordingly and even harmonics can be further reduced. Second, the IL-BUF acts as a buffer and a filter [6], which is identical to LF-ILFM. Therefore, the IL-BUF and the LF-ILFM have the same frequency response and harmonic-filtering property. From the simulation, the IL-BUF can achieve an additional 30dB HRR, and the overall HRR from LF-ILFM plus IL-BUF reaches 65dBc. The schematic of the LF-ILFM and IL-BUF is shown in Fig. 18.1.3, consisting of a dual-resonance load to increase the locking range (LR) to 1.4GHz, and a 3-bit switch capacitor array to cover any PVT variation. The 7th harmonic then goes to a ×5 HF-ILFM.

A current chopper [6] is adopted as a high-efficiency harmonic generator. As shown in Fig. 18.1.3, on each side of the injection devices, a differential signal is fed to the stacked transistors and chops the drain current to generate a harmonic-rich current. The level of each harmonic can be tuned by changing the bias of the injection transistors. Therefore, by properly designing the biasing point, we can generate a high-level 35th harmonic, and significantly suppress the 7th, 21st, and 49th harmonics. The generated 35th harmonic finally goes into the HF-ILFM to achieve the ×35 frequency multiplication. Similarly, the HF-ILFM has a dual-resonance load to increase the LR to around 10GHz. Since the undesired harmonics from the HF-ILFM are out-of-band, they will be removed by the following RF stages.

The chips are fabricated in a 40nm CMOS process. The TX chip has a 1.9×0.45mm^2 area, and the RX chip area is 1.9×1.26mm^2. The power consumption for the TX and RX chips is 160mW and 420mW, respectively. Figure 18.1.4 shows the measured LO performance, and all the spectrums are captured after an external downconversion mixer. The HRR is 55dBc at 81.2GHz, and the output PN curve tracks the reference PN well from 1kHz to 100MHz offset, with -112.4dBc/Hz at 1MHz offset. This proves that the proposed frequency multiplier generates negligible PN compared to the reference, and it is suitable for a coherent radar system. The FMCW chirp performance is also measured, and we can generate an ultra-fast chirp with 1.17GHz/μs chirp-rate and 0.34% maximum frequency deviation. Note that the maximum chirp-rate is limited by the signal generator. The maximum achievable chirp bandwidth (BW) is 5.2GHz.

The TX and RX chip performance are shown in Fig. 18.1.5. The TX has 10dBm output power and covers an 80-to-90GHz band by switching the LF-ILFM bands with more than 6GHz BW in each sub-band. The HRR is above 50dBc from 80.5 to 82.5GHz, and above 45dBc from 80.5 to 86GHz. The RX has a 20dB gain with 8GHz BW, 8.3dB noise figure (NF), and a wideband return loss. The measured input P_{1dB} is -0.7dBm at 20kHz IF (out-of-band), and -7dBm at 1MHz IF (in-band). The I/Q phase mismatch in the RX, measured at 1MHz IF, is less than 5 degrees.

Figure 18.1.6 compares the chip performance with prior art. Our chip uses a 2.4GHz LO synchronization frequency, which is >8× lower than the state-of-the-art, enabling superior scalability to create large TRX arrays. Meanwhile, we achieve the fastest FMCW chirp (>3×) with good linearity. Additionally, due to the use of an N-path mixer-first receiver, our RX shows 6dB better input P_{1dB}, comparable NF, and much lower power consumption than other architectures thereby enabling cost-effective, highly scalable, and high-performance next generation radar perception systems with improved angular resolution for ubiquitous autonomous sensing applications.

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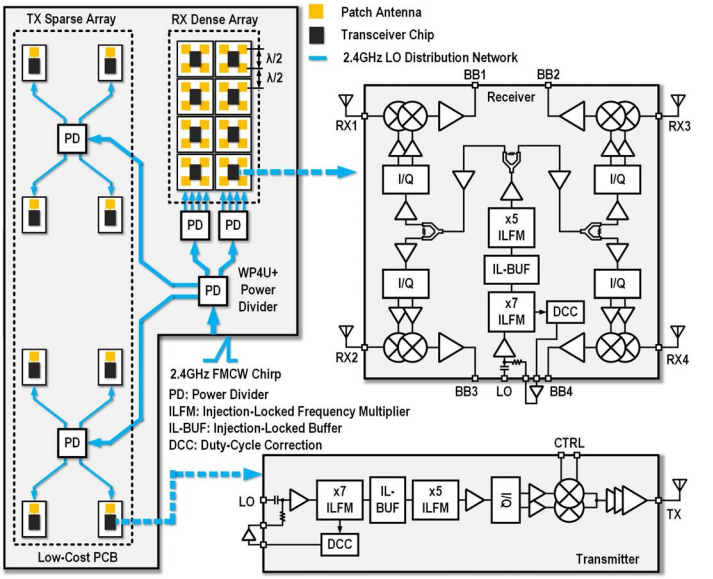

Figure 18.1.1: Conceptual scalable MIMO array and PCB assembly method. The block diagram of the W-band FMCW receiver, and the transmitter.

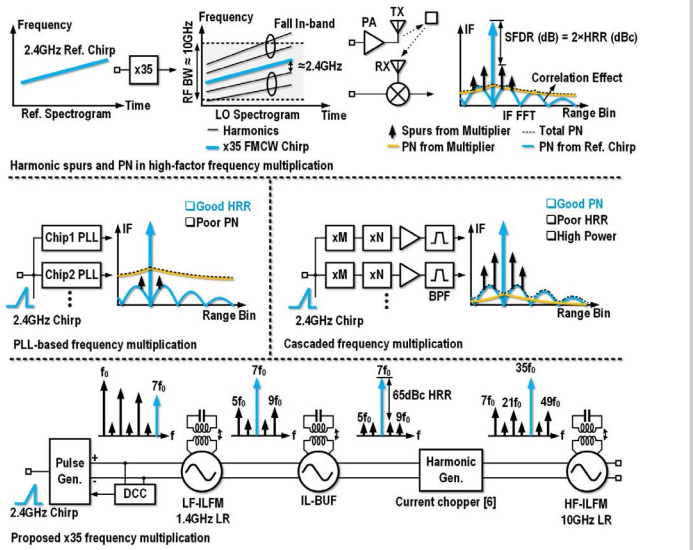

Figure 18.1.2: Challenges in concurrently achieving high harmonic-rejection ratio (HRR) and low phase noise (PN) in typical high-factor frequency multipliers for high SFDR radar systems (top), and our proposed approach (bottom).

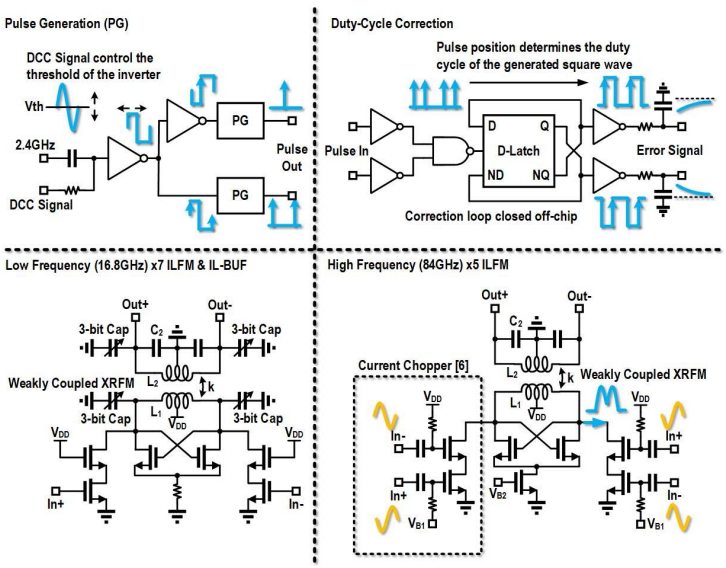

Figure 18.1.3: Block diagrams and schematics of building blocks in LO generation.

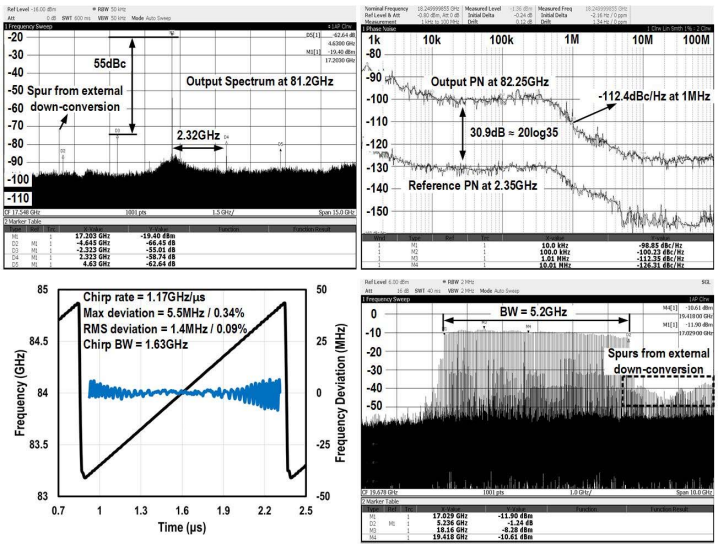

Figure 18.1.4: Measurement results of TX output spectrum, PN, and chirp performance for fast and wideband chirp.

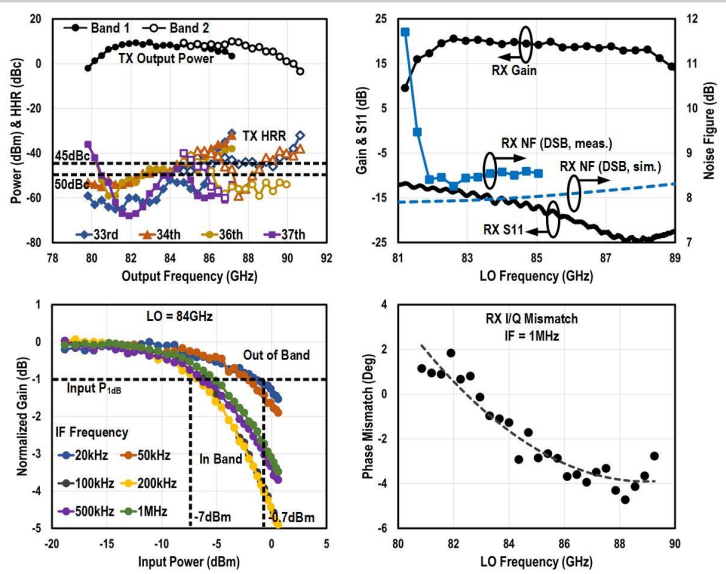

Figure 18.1.5: Measurement results of TX output power, HRR, RX gain, NF, S11, input P_{1dB}, and I/Q phase mismatch.

	JSSC'20 Tsinghua [7]	ISSCC'21 TI Gen2 [2]	ISSCC'19 Uhnder [8]	ISSCC'21 CETC [3]	JSSC'21 Denso [9]	This Work
Process	65nm CMOS	45nm CMOS	28nm CMOS	65nm CMOS	40nm CMOS	**40nm CMOS**
# RX/# TX	3/2	4/3	8/12	4/3	8/3	**4/1**
Frequency (GHz)	76-81	76-81	76-81	76-81	76-77	**80-90**
LO Sync. Freq. (GHz)	40	20	-	40	-	**2.4**
LO Multi. Factor	2	4	5	2	-	**35**
Modulation	FMCW	FMCW	PMCW	FMCW	FMCW	**FMCW**
PN (dBc/Hz) @ 1MHz	-87	-93	-110	-90	-91	**-112**
Max. Chirp BW (GHz)	4	5	-	7.2	1	**5.2**
Chirp Rate (MHz/μs)	133	266		340	40	**1170**
Chirp Linearity	0.11%	0.06%	-	0.66%	0.06%	**0.34%**
TX Pout (dBm)	13.4	12.1 – 13.2	8.8*	11.8 – 14.5	11 – 14.1	**10**
RX SSB NF (dB)	15.3	12 - 13.8	16*	12.2 – 20	8.7 – 14	**11.3**
RX OOB P_{1dB} (dBm) [20kHz blocker]	-8.5	-10	-6.7	-7	-7.4	**-0.7****
Power Consumption per Channel (mW)	184	500	475	510	290	**160 (TX) / 105 (RX)**
Chip Area (mm^2)	7.29	22	71	33.6	46.2	**0.86 (TX) / 2.4 (RX)**

* At package reference plane, 125°C.
** Measured by feeding a CW tone below the lowest HPF cut-off frequency (20kHz).

Figure 18.1.6: Summary and comparison table.

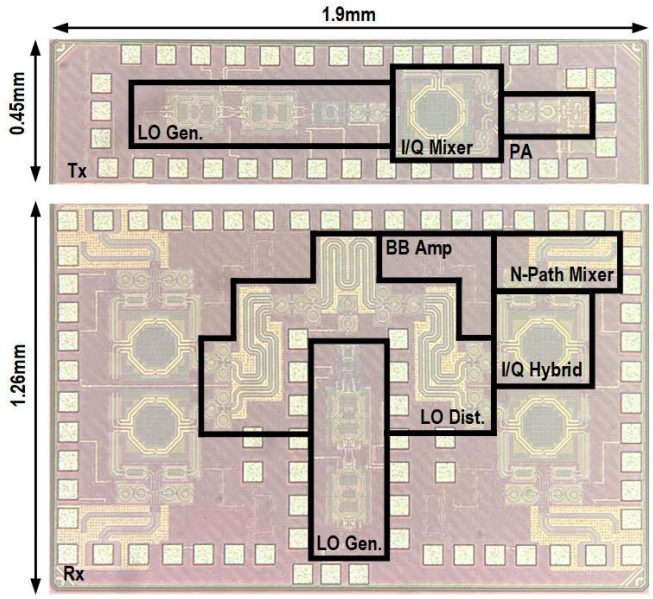

Figure 18.1.7: Die micrograph.

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