EE114/EE214A, Autumn 2016

Course Information

General Information
Course: EE114/EE214A, Fundamentals of Analog Integrated Circuit Design
Time: Tue & Thu, 10:30 am – 11:50am Location: Skillaud
Units: 3-4 (Undergraduates must take EE114 for 4 units)
Prerequisite: EE101B
Website: https://canvas.stanford.edu/courses/47758

Check website for updated information regarding office hours, review sessions etc. We will use this website for posting lecture notes, homeworks, and grades. Major announcements will be emailed. Please plan ahead and make use of TA office hours in order to resolve other issues and use TA emails mainly for simple and quick questions with "EE114/EE214A" in the email's subject. Piazza will also be available for student-to-student assistance although it won't replace office hours since the teaching staff will sparingly review the activity on Piazza. However, this doesn't mean you can use Piazza in order to "check" answers to homework questions, as we expect everyone to abide by Stanford's honor code.

Course Description
Analysis and simulation of elementary transistor stages, current mirrors, supply- and temperature-independent bias, and reference circuits. Overview of integrated circuit technologies, circuit components, component variations and practical design paradigms. Differential circuits, frequency response, and feedback will also be covered. Performance evaluation using computer-aided design tools.

Instructor
Prof. Amin Arbabian
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Administrator
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Teaching Assistants
Miaad Aliroteh (miaad@stanford.edu)
Ajay Singhvi (asinghvi@stanford.edu)

Recommended Texts
1. B. Murmann, *Analysis and Design of Elementary MOS Amplifier Stages*, National Technology and Science Press, to appear in 2011.
2. P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley, 2009

Grading
1. Homework – 25% (Drop lowest score)
2. Midterm Exam – 25%
3. Project – 15%
4. Final Exam – 35%

Piazza
Occasionally we will be using Piazza as our online forums in order to posting clarifications to assignments. However, it is meant to be a forum for students to interact among themselves, with minimal participation by the TAs or course instructor. **Extra credit** will be given to the students with the highest participation in

answering questions. We highly recommend attending at least one TA office hour session per week in order to clarify any issues you have with assignments.

Honor Code
Please do not treat Piazza as a way of "checking" answers to homework questions, as we expect everyone to abide by Stanford's honor code. Just as a reminder, the honor code applies to all parts of all classes; more information can be found at:
https://communitystandards.stanford.edu/student-conduct-process/honor-code-and-fundamental-standard#honor-code

Homework Submission
Homework will be handed out on Thursday and will be due the following Thursday 4pm sharp. On-campus students can submit their homework in class or in the drop-box located on the second floor of Paul G. Allen Building. SCPD students should submit their homework via the regular SCPD channel before the deadline stated on the handout.

Course Schedule (Tentative)

Week 1	9/27, 9/29	Introduction, IC Technology, Long Channel MOS Model, Common Source Amp, Small Signal Model	HW1 out
Week 2	10/04, 10/06	Gain and Bias considerations, finite output resistance, Intrinsic capacitance, Extrinsic Capacitance	HW1 due, HW2 out
Week 3	10/11, 10/13	Miller, ZVTC Dominant pole approx., Backgate effect, Common Gate Stage	HW2 due, HW3 out
Week 4	10/18, 10/20	Common Drain Amp., Current Mirrors, Voltage Biasing Considerations, Differential Pair (Intro.)	HW3 due, HW4 out
Week 5	10/25, 10/27	Differential Pair, PVT variation, Supply Insensitive Bias current generation, Intro to BJT	HW4 due, HW5 out
Week 6	11/01, 11/03	Bandgap References, MIDTERM (Time and Location TBD)	Project out
Week 7	11/08, 11/10	Multi-stage amplifiers, Intro to Feedback, Design Problem Examples.	HW5 due
Week 8	11/15, 11/17	Feedback with 2-port Networks, Practical Feedback,	HW6 out
Week 9	11/22, 11/24	Thanksgiving Recess (No classes! We recommend getting started on the Project early!)	
Week 10	11/29, 12/01	Feedback and Stability, Return Ratio	HW6 due, Project due, HW7 out
Week 11	12/06, 12/08	Feedback and Port Impedances	HW 7 due
Week 12	12/14	FINAL EXAM (12:15pm-3:15pm, Location TBD)	