Oscillators (and VCO)

Oscillations and Voltage-Controlled Oscillators

- Feedback perspective $A = a/(1 - af)$, if $af = 1$ we get infinite gain... or oscillations
- From EE 122 the phase-shift oscillator specifically uses series-parallel RC network to:
  - Make $|f| = 1/|a|$ and
  - Guarantee exact 0-degree phase shift
- Timing-based oscillations--this can be “ring oscillator” type or “charge-discharge” (of C) type
- Transistor level oscillations (which we’ll do now)

This discussion, while couched in terms of oscillators, has relevance to amplifiers as well--often in terms of considering how to make the amplifier NOT oscillate.

Also, please refresh your memory about the general feedback expression (aka EE113/101B) since it is critical when considering impedances as well as gain expressions.

There is LOTS to say about kinds of oscillators--phase-shift versus relaxation-, ring-type etc.

Also, it is important to differentiate between sinusoidal oscillations (a single “tone”) versus (ring- and) relaxation-type oscillators that create triangle or square-wave oscillations.

In lab you will have a chance to consider both a sinusoidal oscillator (the so-called “Colpitts” oscillator, named after its inventor) and a relaxation-type oscillator.
Quick reminders from EE122 (and EE102/101B about the s-plane plot) concerning the “phase shift” oscillator.

This oscillator has two key kinds of feedback:

1) The classical R1-R2 “negative” feedback, which gives a voltage gain as indicated and

2) Feedback around the positive loop where the two [square boxes] indicate an R-C (or L-R-C) network that is frequency selective and has a unique frequency where the phase-shift is exactly zero.

At this frequency (by design) the attenuation of the R-C is balanced by the gain of the R1-R2 block such that oscillations are sustained.

In the s-plane we want the poles to be located exactly on the $j\omega$ axis—if they are in the Left Half Plane (LHP) the oscillations will decay away and if in the Right Half Plane (RHP) the oscillations will grow without bound…
Timing-based Oscillators (see Grebene)

Timer Circuits:
- Schmitt Trigger
- 555 IC
- Many others...

\[ I = C \frac{dV}{dt} \]
\[ \frac{C \Delta V}{I_x} = T_x \]

“x” is the portion of the total period for which the respective “Ix” is in control

Now let’s turn our attention to the “relaxation-type” oscillator, shown schematically here as simply a storage element that is being charged and discharged by two current sources.

Basically, there are many chips that employ this kind of oscillator; possibly the one most familiar to you would be the 555 “timer chip” where all you have to do is select the capacitor (and one resistor) to create such oscillations.

The capacitor’s governing equation (differential form) is shown.

For a constant-valued capacitor we can use \( \Delta V \) and \( \Delta T \) and for each portion of the charging (or discharging) of the capacitor \( \Delta T \) becomes \( T_x \).

Hence, the fraction of the period called out as \( T_x \) is directly proportional to \( C \) and \( \Delta V \) and inversely proportional to \( I_x \).

We can make the wave forms symmetric or asymmetric by changing the values for \( I_x \) on each portion of the waveform.

Finally, although not written on this slide, the frequency of oscillation is given by the INVERSE of the sum of \( T_1 + T_2 \).
The following slides come from a supplemental handout taken from Alan Grebene’s book Bipolar and MOS Analog Integrated Circuits. Alan was the lead designer who created the 555 and related products. 

This figure shows schematically the two current sources that charge and discharge the capacitor $C_1$. The Schmitt trigger circuit (an old friend from EE122?) sets the voltage excursions over which the voltage $V_{O1}$ will travel (i.e. $\Delta V = V_B - V_A$).

During the charge-up period ($T_1$) the lower current source is assumed to be “off” so that the slope of $V(t)$ is determined only by $I_1$. Once the voltage reaches $V_B$ the current source $I_2$ turns on (and its value is greater than $I_1$) so that the discharge period ($T_2$) is determined by $I_2 - I_1$.

A few more details, including the equations to go with the above discussion, are shown on the next figure.
Simple reminder about the Schmitt trigger…It provides a digital (logic H and logic L) output with a hysteresis in the transitions going L->H and H->L determined by $V_A$ and $V_B$.

In this figure $V_{HI}$ corresponds to $V_B - V_A$.

The two fractions of the total period, $T_1$ and $T_2$, are determined by the capacitor and current source values (as shown in the schematic on the previous page).

The resulting frequency of oscillation is given by the inverse of the sum of the two times as shown.

The above discussion has been rather general in terms of allowing the two currents to have arbitrary values.

The next slide gets down to one specific application where in fact the current is “diode steered” such that $I_1 = (I_2 - I_1)$.

\[ T_1 = \frac{(V_B - V_A)C_1}{I_1} \]

\[ T_2 = \frac{(V_B - V_A)C_1}{I_2 - I_1} \]

\[ f = \frac{1}{T} = \frac{1}{T_1 + T_2} = \frac{I_1}{(V_B - V_A)C_1} \left( 1 - \frac{I_1}{I_2} \right) \]
Implementation of Current Sources
(and “diode steering” of currents)

This schematic shows an abstracted view of what you will be using in the 566 chip.

Basically, when $S_1$ is OPEN the current $I_1$ can only flow through $D_2$ and charge-up $C_1$

When $S_1$ is CLOSED, the current mirror (a so-called Wilson Mirror after it’s inventor, George Wilson and former Motorola and Tektronix designer) pulls the current $I_1$ through $D_1$ and the in turn $Q_2$ forces that same current to flow which then discharges $C_1$

In the process you can easily convince yourself that $D_2$ must be off--basically, once $S_1$ “offers” a lower potential path for $I_1$ to flow through, the current goes that way and the potential at the “cathode” side of the diodes drops to that value [to be discussed a bit more in class…both using this figure and probably the real schematic for the 566 :)]

From your perspective as USER of the 566, the control voltage ($V_C$) sets the current value for $I_1$ and you have the choice of selecting $C_1$ to set the frequency of oscillation.

$V_c$ can be either (dc) or $V(t)$--the former giving a single frequency and the later giving a “frequency modulated” (or FM) signal
This is the schematic of the 566.
The key blocks such as the two current sources ($I_1$ and $I_2$) are indicated along with the Schmitt Trigger etc.

In commerical ICs there are LOTS of details that need to be considered to have the chips work over variations in temperature, supply voltages etc.

Hence, these are NOT your most basic current sources, mirrors etc. and extra devices are added to perform a variety of “compensations”

We will not try to talk about any of this in detail. But, hopefully you clearly see the basic block-level sub-circuits and appreciate how your control over it reaches inside the chip to control the internal variables.
Now for a “more challenging” Oscillator

Colpitts Oscillator (Analysis and Design):
The following is a combination:
• First-order, small-signal analysis (Dutton)
• Improved “large signal” version (T. Lee, ala EE 314)

Common Base Amp.:
• Biasing like CE but!
• BIG Cap at base=ac ground
• Cap divider from collector back to emitter (we'll talk more about “tuned circuits” soon)
• TANK circuit at collector
Bottom-line:
CB=>non-inverting GAIN stage + Cap divider closes loop with \( \phi = 0 \) (I.e. oscillations)

This is the beginning of our discussion of the Colpitts oscillator, a truly elegant and MINIMAL circuit.

You do have to remember (or quickly learn) that the basic gain block is a common base (CB) amplifier.

[the “ac ground” at the base is actually a large capacitor]

The bias is a voltage divider to the base lead which sets that voltage; the current source could be simply a resistor

[if it was a resistor, the current would be \( (V_B-V_{BE})/R \)--assuming the bottom ground is a real ground and that there is only a +V supply]

The gain (simple small signal model) between the emitter and collector is (non inverting) \( +g_m R(\text{equiv. ac load})>>+1 \)

That voltage gets “fed back” from collector to the input via a capacitive divider…what’s that you say? The following equation explains:

\[
V_{\text{emitter}} = V_{\text{collector}} \cdot \left[ \frac{1/sC_2}{1/sC_1 + 1/sC_2} \right] 
\]

\[
= V_{\text{collector}} \cdot \left[ \frac{C_1}{C_1 + C_2} \right] 
\]
OK, let’s work through the details…

This figure shows the transformation of the circuit into its equivalent “small signal” equivalent.

Note that the arrow shows where the “input” to the CB is and viewed as a “voltage” input this appears across the base-emitter junction (and the $r_\pi$ of the circuit)

The impedance seen here is NOT $r_\pi$! What is it? (remember the reflection rules? It is reduced by $1/(\beta+1)$!)

Now, since we haven’t done all the “tuned circuit” part of things yet, we initially will give you the parameters needed for lab in order to get oscillations at the desired frequency.

The following is more of the DETAILS of the analysis and design of the Colpitts. It will make much more sense after we have worked (in detail) on the tuned circuits part…

So, here goes with the analysis (and discussion).
Since we end up doing all the analysis in terms of voltage and for large signal we can not simply use the small-signal $g_m$, the circuit shown in the bottom right corner is a LARGE SIGNAL equivalent $R_{in}$ and $G_m$

The input (loop) has been broken and we will compute the “loop gain” by inserting a voltage at $V_1$ and do the analysis “around the loop” to see what voltage comes back. [Comment on loading at $C_2$]

Clearly, $G_m V_1$ is the current that “drives” the load. There is an equivalent (complex, frequency selective) impedance seen at $V_{tank}$

And…

That voltage will be “divided down” by the capacitive divider ratio “n” $[=C_1/(C_1+C_2)]$

Hence, the overall “loop gain” will be:

$$A_{loop–gain} = G_m \cdot Z_{tank}(\omega_{resonance}) \cdot n$$
Assume a V1:

\[ V_{\text{tank}} = +G_m V_1 Z_{\text{tank}} \]

at resonance, \( Z_{\text{tank}} = R_{\text{eq}} = R_{iT} \parallel R \)

(where \( R \) is all other resistances* and \( R_{iT} \) comes from
the impedance transform of \( R_{\text{in}} \) based on \( C_1 \) & \( C_2 \))

\[ V_o = n V_{\text{tank}} = \left[ \frac{C_1}{C_1 + C_2} \right] V_{\text{tank}} \]

and, if \( V_o = V_1 \) we will have condition for oscillations

*Footnote: This notation follows T. Lee (copy from text attached).

This slide simply walks through some of the intermediate steps that
go with the words shown on the “notes” part of the previous slide.
A KEY (and at the moment a bit mysterious) part of this slide and
portions of ones that follow is the “Impedance Transformation” part
of things.

Basically, just as the capacitive “divider” divides down the voltage
(\( V_{\text{tank}} \)), it also “transforms” up the impedance that appears across \( C_2 \)
That is, if the input impedance seen at \( V_1 \) is \( R_{\text{in}} \), the series \( C_1 \)-\( C_2 \)
combination makes that resistance appear much larger as seen at
the \( V_{\text{tank}} \) node…(more to come soon in the next lectures)

Bottom-line:

Even if \( R_{\text{in}} \) is small (as we expect for the input of a CB stage), it’s
value gets “Impedance Transformed” up to a larger value so that
the “loop gain” can be greater than unity--the condition needed to
sustain oscillations.
At the highest level, we can use simple feedback theory to emphasize a couple of points:

\[ a = \frac{G_m R_{eq}}{f = \frac{C_1}{C_1 + C_2}} \]

af = 1 \rightarrow denominator is zero

Or..

af > 1 and the phase is such that we have POSITIVE feedback (the case for the Colpitts)

*Footnote: It turns out that, as shown in Fig. 16.6 (T. Lee book) the current flow in the device is highly non-linear (spiked in time as VBE turns on) and we really can’t use normal small-signal parameters for Gm. How to cope with that problem is discussed in Sect. 16.3.2 of T. Lee text (Ch.16)

This slide simply reiterates what we said at the beginning of lecture in slide one.

If “af” goes to unity and has phase such that it cancels the “1” in the feedback equation, we have the conditions for oscillations.

There are various “pointers” to sections/figures in the Tom Lee book on CMOS RF.

That book and these sections are really awesome in terms of presenting simple conceptual pictures and nice computations that give quantitative details about the oscillations, based on a large signal model that was constructed above. [Form of model is like the small-signal…Comments in class]

Basically, I’ll very quickly highlight some of the points from the sections in the CMOS RF book of Prof. Lee.

Good News: Even if you feel “bogged down” in the math and derivation [next pages], the final equations/results give you a quick estimate of how large the expected voltage oscillations will be for the Colpitts and how to control them.
This slide won’t make much/any sense unless you READ the sections from CMOS RF and you are “up to speed” on impedance transformations.

The top [bracketed] set of equations tell us what the equivalent tank impedance will be--the parallel combination of the R that’s there due to the inductance and \((1/G_m)(1/n^2)\)

This product of TWO terms is \(R_{in}\) times the transform. Since \(n<1\), that means that \(1/n^2\) will be a rather LARGE number.

To achieve large loop-gain we want \(R||R_{iT}\) to still be large.

The middle part about “voltage gain” is rather obvious, with the exception of the \((2I_{tank})\) term (again…read the handout!)

Finally, the “Closing the Loop…” part is some detailed equation hacking. It is not hard but it’s not obvious either…. I’ll discuss in class a bit as time allows.
\[ V_{\text{tank}} + n \cdot R \cdot 2I_{\text{bias}} = 2I_{\text{bias}} R \]
\[ \therefore V_{\text{tank}} = 2I_{\text{bias}} R \cdot (1 - n) \]

**Other notation:**

\[ C_{eq} = \frac{C_1 \cdot C_2}{C_1 + C_2}; \quad \omega = \frac{1}{\sqrt{L \cdot C_{eq}}}; \quad n = \frac{C_1}{C_1 + C_2} \]

This is the bottom-line result, giving the final tank voltage in terms of the bias current, R and the voltage divider ration n.

The final (DESIGN) result is the [boxed] equation for \( v_{\text{tank}} \) in terms of:

1) \( I_{\text{bias}} \)

2) \( R \) (the “load” at resonance provided by the “tank” circuit) and

3) (1-n) which is determined by the capacitive divider ratio

Hence, if you want larger tank voltages you need to increase \( I_{\text{bias}} \) or \( R \) and make “n” much smaller than unity (clearly you can only get so much from the “n” term vis a vis the bias current or the quality of the L-C components (which in turn controls the R)

Again, in thinking about and planning for lab, at this point we will have already “designed” the Colpitts. Your job will be to hook it up and make it oscillate--sometimes frustrating (like fishing, there are elements of both skill and luck involved…listen carefully to your TA/mentors :).
In lab you will be implementing the Colpitts and related circuitry for making it a “Voltage Controlled Oscillator” (VCO) by means of a Varactor (Variable Reactor) Diode--basically a voltage-variable capacitance (the C(V) of the diode in reverse bias--one of my favorite uses for diodes from EE111 :)

I’ll leave the discussion of this figure to the text from the kit (per the next slide)

Hopefully after the lab and all your hard-won experience, reading this discussion will make LOTS of sense and you can even explain it to your little brother or sister who will certainly want to follow in your footsteps as a gEEk…building such kits to prepare for their future career path.
As stated in the last slide, I won’t reiterate the above discussion. However, I would like to point out one key feature of this design that may indeed be important (and useful in the future)

There is a single-chip voltage regulator used in this design to keep the Varactor voltage sable.

Note in the text that this is considered to be important in achieving “frequency stability”

As you will see as we get into the SPAMMING exercises, the tuning (and drift) of your oscillators is a MAJOR challenge.

[More to come on all this]