OPERA: OPtimization with Ellipsoidal uncertainty for Robust Analog IC design

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Introduction

- Design-manufacturing interface is becoming more and more complex
- RF and analog integrated circuits are very sensitive to process variation
Variability in DSM technologies is increasing

Large-scale variation results in lower product yield

Control performance variability in early design stages

[Graph showing variation in VTH, TOX, W, L, H, and ρ across different L_eff (nm) values from 250 to 70 nm.]

[Nassif 01]
Traditional Corner-Enumeration Optimization

**Corner-enumeration worst-case optimization**
- Most widely used robust design technique
- Uncertain parameters are often assumed to have independent uniform distributions
- Design is optimized for all corners of a $\pm 3\sigma$ tolerance box

**Problems with corner-enumeration optimization**
- Often *ignores correlation* between process parameters
- Problem size increases *exponentially* in number of uncertain parameters
- *No guarantee* for parameter points inside the $\pm 3\sigma$ tolerance box
- Design for all corners could result in *over-design*
Sources and Statistics of Variability

- **Environment variations**
  - Power supply voltage
  - Temperature
  - Noise coupling

- **Model environmental variations by Uniform distributions and capture their variability by polyhedron**

- **Manufacturing variations**
  - Device
  - Interconnect

- **Model manufacturing variations by Normal distributions and capture their variability by ellipsoid**
Capturing the process variation

- Process variation statistics are characterized by joint-pdf [Nassif’01]
  - Independent Gaussian random variables
  - Correlated Gaussian random variables

- Multivariate Gaussian Distribution \((\mu, \Sigma)\)
  \[
p_{x}(X) = \frac{1}{(2\pi)^{n/2} |\Sigma|^{1/2}} \exp \left\{ -\frac{1}{2} (X - \mu)^T \Sigma^{-1} (X - \mu) \right\}
  \]

- Equidensity contour is concentric ellipsoid
  \[
  U = f(\mu, \Sigma, r) = \left\{ X \in \mathbb{R}^n \mid (X - \mu)^T \Sigma^{-1} (X - \mu) \leq r^2 \right\}
  \]

- Probability has a chi-square distribution with degree \(n\)
  \[
  \text{Prob} \left( u \in U \right) = F_{\chi_n^2} (r^2)
  \]
OPERA Concept

GP Modeling of Analog Circuit + Process Variations

Variance linked to mean
Variance not linked to mean

Stochastic GP with Joint Probability

Specification on Yield

Robust GP with Ellipsoidal Uncertainty

Capture Process Variations by Ellipsoid (Chi-square distribution)

Robust Design with Guaranteed Yield
Robust Optimization Approach

Robust geometric programming†

- Robust GP incorporates a model of data uncertainty and optimizes for the worst-case scenario under the model
- Computation time increases linearly in number of uncertain parameters

Design for variability via robust GP:

- Many analog IC design for variability problems can be cast as robust GPs
- Handles correlated statistical variations in both process parameters and design variables
- Can carry out robust designs with required yield bound
- Results in less over-design (compared with corner-enumeration optimization)

† More details can be found in “Tractable Approximate Robust Geometric Programming”, revised for publication, May 2005
Modeling Process Variations

**Variance-linked-to-mean variation**

- **Relative variations** (e.g. $\Delta R/R$, $\Delta C/C$), i.e. variance is proportional to mean
- Model the variations in process parameters by

$$\frac{\delta p_i}{p_i} \sim N \left(0, \sigma_i^2\right), \ i = 1, \ldots, q$$

**Variance-not-linked-to-mean variation**

- **Absolute variations** (e.g. $\Delta W$, $\Delta L$, $\Delta V_{th}$), i.e. variance is independent of mean
- Model the variations in both design variables and process parameters as

$$\delta p_i \sim N(0, \sigma_{p_i}^2), \ i = 1, \ldots, q, \quad \delta x_j \sim N(0, \sigma_{x_j}^2), \ j = 1, \ldots, n$$
Lognormal approximation

- Narrow normal distribution can be approximated as lognormal distribution
- Most process parameter variation satisfy this condition (e.g. tox)

\[
\begin{align*}
\mu &= 4.45 \text{nm}, \\
\sigma &= 0.1 \text{nm}
\end{align*}
\]

Effective tox (nm) fitting normal distribution with lognormal distribution

\[
\text{Normal distribution } (\mu, \sigma) \quad \text{Lognormal distribution } (\log(\mu), \sigma/\mu)
\]

Tox (4.45nm, 0.1nm)
Fitting error 1.3%

\[\mu = 4.45 \text{nm}, \sigma = 0.1 \text{nm}\]
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Ring Oscillator Design Example

- 5GHz Ring Oscillator design example
- IBM 7HP 1.8V 0.18\(\mu\text{m}\) BiCMOS process
- Design Variables:
  - \(W_{\text{eff}}, L, \Delta V\)
- Design objective and constraints:

\[
\begin{align*}
\text{Minimize} & \quad \text{Power} \\
\text{Subject to} & \quad \text{Phase Noise} \leq \text{PN}_{\text{max}} \\
& \quad f_{\text{resonant}} = f_0
\end{align*}
\]
Optimization results (90% yield bound for robust GP, Freq: 5±1 GHz):

<table>
<thead>
<tr>
<th>Design Variables</th>
<th>GP Design</th>
<th>Robust GP Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weff</td>
<td>4.53µm</td>
<td>6.68µm</td>
</tr>
<tr>
<td>Length</td>
<td>0.26µm</td>
<td>0.24µm</td>
</tr>
<tr>
<td>ΔV</td>
<td>0.42V</td>
<td>0.387V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Specifications</th>
<th>GP Design</th>
<th>Robust GP Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>1.87mW</td>
<td>2.59mW</td>
</tr>
<tr>
<td>Yield</td>
<td>50%</td>
<td>≥ 90%</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-100dBc/Hz</td>
<td>-101dBc/Hz</td>
</tr>
<tr>
<td>Frequency</td>
<td>5GHz</td>
<td>4.85GHz</td>
</tr>
</tbody>
</table>

Robust design achieve better yield with higher design cost
Monte Carlo Verification

- Actual yield is estimated by Monte Carlo analysis with 10K samples.

- Optimization without considering process variation (i.e. nominal design) might have very low yield (50% in this example).

- Robust GP design achieved guaranteed yield $\geq 90\%$.
Design Cost vs. Yield Requirement

- Trade-off curve of power consumption (design cost) versus yield requirement
- Design cost increases when yield requirement increases

Very high design cost to achieve yield approaching 100%
Voltage-Controlled Oscillator Design Example

- 2.1GHz LC VCO design example
- Hitachi SiGe BiCMOS process using 90GHz $f_T$
- NPN
- Differential VCO is equivalent to a tank model
VCO Experiment Setup

**Design Variables:**
- \( I_{\text{bias}}, g_{\text{tank}}, C_{\text{tank}}, L, V_{\text{sw}} \)

**Design objective and constraints:**
- Minimize Power
- Subject to Phase Noise \( \leq PN_{\text{max}} \)
- Loop Gain \( \geq LG_{\text{min}} \)
- \( L_{\text{tank}} \cdot C_{\text{tank}} \cdot \omega^2 = 1 \)
- \( V_{\text{sw}} \leq V_{\text{dd}} \)
- \( V_{\text{sw}} \leq I_{\text{bias}}/g_{\text{tank}} \)

**Design Uncertainty:**
\[
\left( \frac{\Delta C_{\text{tank}}}{C_{\text{tank}}}, \frac{\Delta g_{\text{tank}}}{g_{\text{tank}}}, \frac{\Delta L}{L} \right) \sim N(0, \begin{pmatrix}
\sigma_1^2 & \sigma_{12}^2 & \sigma_{13}^2 \\
\sigma_{21}^2 & \sigma_2^2 & \sigma_{23}^2 \\
\sigma_{31}^2 & \sigma_{32}^2 & \sigma_3^2
\end{pmatrix})
\]
VCO optimization results

- Robust GP yield bound:
  - Yield bound can be set by adjusting the ellipsoid radius

- Corner selection — vertices of polyhedron
  - Confidence ellipsoid in the robust optimization is inscribed in this polyhedron

- Optimization results (for 90% yield bound, Freq: 2.1±0.4GHz)

<table>
<thead>
<tr>
<th></th>
<th>Robust optimization</th>
<th>Corner - enumeration optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_bias</td>
<td>2.41mA</td>
<td>2.72mA</td>
</tr>
<tr>
<td>C_tank</td>
<td>1.33pF</td>
<td>1.26pF</td>
</tr>
<tr>
<td>g_tank</td>
<td>0.894mS</td>
<td>1.018mS</td>
</tr>
<tr>
<td>L</td>
<td>2.83nH</td>
<td>2.82nH</td>
</tr>
<tr>
<td>Vsw</td>
<td>2.5V</td>
<td>2.5V</td>
</tr>
</tbody>
</table>
LC Oscillator design cost vs. yield bound and actual yield

- Yield is estimated by 10K Monte Carlo analysis
- Design cost increase when yield requirement increase
- 20% over design for $\pm 3\sigma$ actual yield in corner-based optimization compared to robust optimization
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Discussions and Conclusions

- Ellipsoidal uncertainty captures both independent and \textit{correlated} process variations.
- \textbf{Yield requirement can be explicitly incorporated as a design constraint.}
- Robust optimization using posynomial equations (requires fewer simulations).
- Guaranteed yield bound by assuring all parameters within the ellipsoid instead of sampling the process variation.
- Handles both parameter and \textit{design variable} uncertainty.
- \textbf{Achieve the same yield with much less over-design} (compared with corner-enumeration optimization).