HIGHLY INTEGRATED 2-D CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

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Abstract— **Two dimensional (2-D) silicon based capacitive micromachined ultrasonic transducer (cMUT) arrays are fabricated efficiently using standard integrated circuit (IC) processing techniques. Furthermore, high density interconnects are implemented using through-chip vias which bring the signal from the front surface of the transducer chip to the back side. The transducer chip then can be flip-chip bonded to a signal processing chip. This results in a very compact two chip hybrid package that can be easily sealed for immersion applications. The electrical interconnects are realized by high aspect ratio vias (50 μm in diameter, 550 um in depth) that are etched into the silicon substrate by a deep reactive ion etcher (DRIE). The vias are then coated by polysilicon which is subsequently doped to achieve good conductivity. The transducer arrays are then built on the front side using the conventional process developed for cMUTs. Measurements indicate that the through wafer vias have a typical resistance of 7 Ω. The parasitic via capacitances are reduced to 2 pF by reverse biasing the p-n junction formed by the n++ doped polysilicon via coating and the near-intrinsic p-type silicon substrate. Ultrasonic measurements on the 2-D array cMUT elements with these interconnects shows more than 100% fractional bandwidth and high sensitivity.**

Keywords— **Ultrasonic transducer array, micromachining, through-wafer interconnect, deep reactive ion etch, flip-chip package**

I. Introduction

Although there have been advances in the fabrication of 2-D piezoelectric ultrasonic transducer arrays, the implementation of an electrical interconnect scheme without any adverse effects on the acoustic performance is still an important problem. Several approaches, such as the use of thick film technology or backing materials with conductive paths have been proposed as solutions [1], [2]. These techniques introduce increased levels of electrical and acoustic cross-coupling, which result in a degraded radiation pattern and impulse response for the transducer array.

The cMUT has emerged as an attractive alternative to conventional piezoelectric ultrasonic transducers in terms of sensitivity and bandwidth [3], [4], [5]. The IC processing techniques used in the fabrication of cMUT arrays also enable one to realize high density interconnects required for 2-D ultrasound arrays. There are several approaches to electronics integration of cMUTs. For a single-chip solution one should develop a cMUT process that is fully compatible with the CMOS fabrication [6]. This can limit the performance of both the electronics and the transducer. In our approach, the cMUTs and their interconnects are fabricated on the same wafer with optimized conditions. The transducer chip can then be flip-chip bonded to the wafer containing the signal processing electronics, which has been fabricated by standard IC process.

In this paper, the fabrication of a 2-D cMUT array complete with the through wafer electrical interconnect is described in detail. Electrical measurements of the series resistance and the capacitance of the through wafer via are presented and compared with theoretical calculations. The impulse response of a cMUT with backside connection is also presented.

II. CMUT Array Fabrication Process

The fabrication of the cMUT with through wafer interconnects involves three main steps. Figure 1 summarizes the fabrication process.

A. Wafer preparation and via drilling

We start with a 500 μm thick double-sided polished p-type < 100 > silicon wafer which is thermally oxidized to 1 μm thick. An array of mini vias with 2 μm diameter are etched through the oxide layer on the front side (Fig. 1-1). Vias of 50 μm diameter are etched from the back side of the wafer using DRIE (STS Limited, UK)(Fig. 1-2). The etch is stopped on the thermal oxide by the back side cooling flow increase due to the leakage through mini vias. A detailed view of the oxide membrane with mini vias on the front surface is shown in the picture of Fig 2. The distance between mini vias is 5 μm and the larger via diameter is 50 μm for this particular case. A 2 μm polysilicon layer is deposited, coating the via walls and wafer surfaces. The polysilicon is then doped using gas phase phosphorus drive-in at 1000°C, yielding a conductive path through the wafer (Fig. 1-3).

B. Active device fabrication

The cMUTs are built on the front side polysilicon, which is patterned into individual islands (Fig. 1-3). First a thin layer of LPCVD nitride is deposited at 800°C as an insulator and an etch stop for the sacrificial etch to be performed later. An amorphous silicon sacrificial layer is subsequently deposited and dry-etch patterned into octagonally shaped islands to define the active transducer cavity regions (Fig. 1-4). The nitride membrane is then deposited by LPCVD, after which vias are dry-etched to allow an access path for the sacrificial etchant. After the cavities have been formed by KOH etching (Fig. 1-5), they are vacuum sealed by LPCVD nitride, which is subsequently selec-

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tively back-etched to achieve the desired membrane thickness (Fig. 1-6). Aluminum is then sputtered and wet-etch patterned to act as the top (ground) electrode.

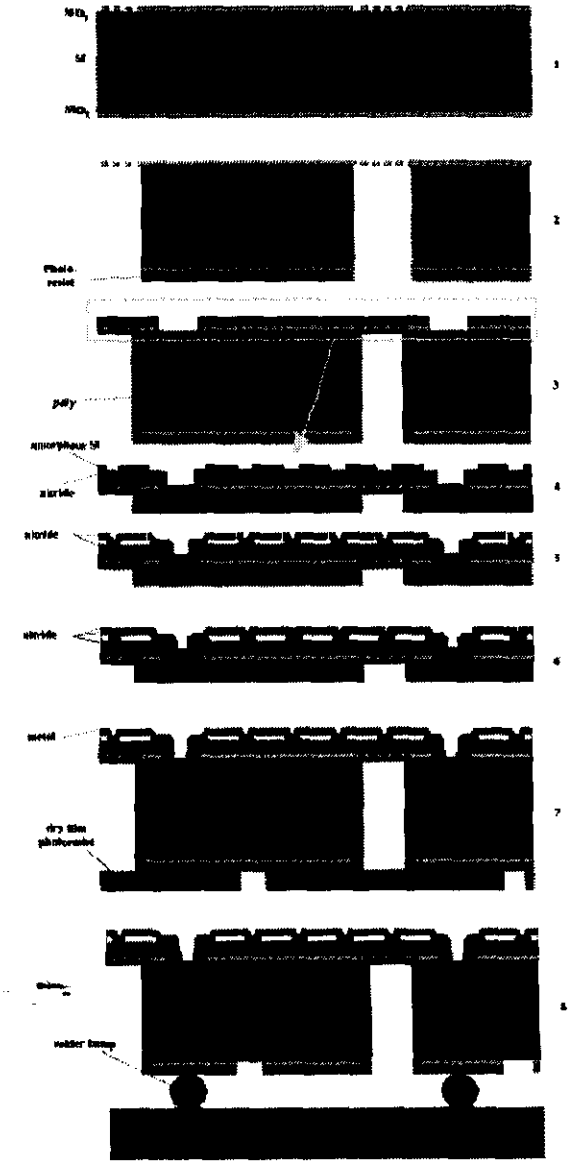

Fig. 1. Process flow for CMUT arrays with through-wafer interconnects.

C. Back end

The back-end processing consists of two special lithography steps on the back side of the wafer, in order to yield the individual contact pads. The presence of the deep vias makes it impossible to deposit photoresist homogeneously on the back side through spin-coating. We use a 30 um thick dry film photoresist (Riston by Dupont) that is laminated over the back side, and that covers ('tents') the via holes, planarizing the surface and allowing a standard photolithography on the back side of the wafer (Fig. 1-7). The backside pads are then defined by polysilicon and oxide dry etch using Riston as a mask. In a final lithographic step, the metal solder bump pads and metal ground strip lines are defined by a Riston lift-off. The chip can now be flip-chipped to a signal processing chip (Fig. 1-8).

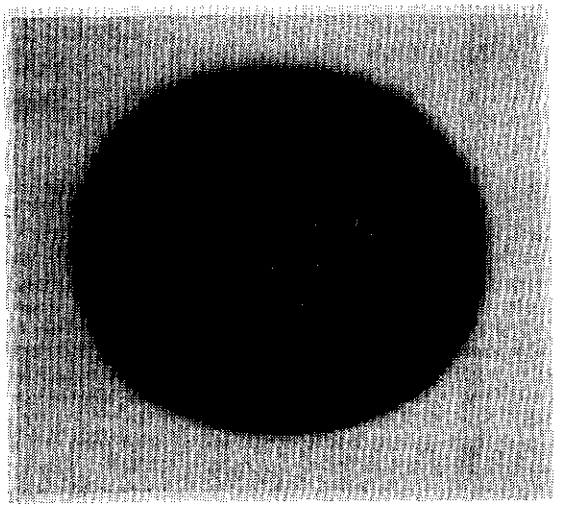

Fig. 2. Mini vias in DRIE etch stop oxide membrane.

Fig. 3 shows the top view of the front side of the array which consists of square elements with 400 μm periodicity. Each element contains 72 membranes with 36 μm diameter. The through wafer interconnect via is seen as a dark circular region. The backside of a similar element is shown in the photograph in Fig. 4. The polysilicon layer covering the through wafer via extends to the backside as a patterned square region. Two metal pads for testing and flip chip bonding are deposited on this polysilicon island. Also seen is the ground metal line surrounding the active signal electrode. The overall view of the 16x16 array from the backside is shown in Fig. 5. The rightmost two rows are covered with metal and use to connect the the ground electrodes in the front and back of the array.

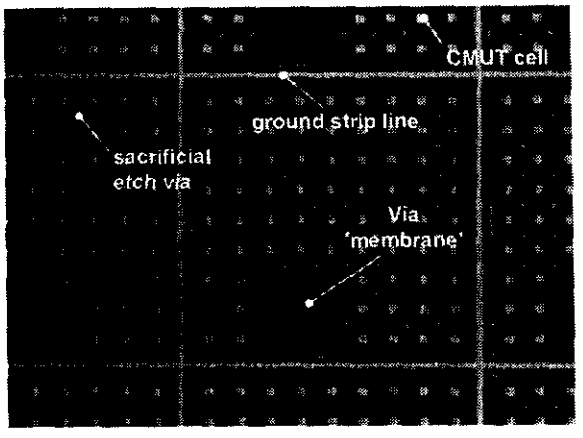

Fig. 3. Front side of CMUT chip; one array element in the center, consisting of 72 capacitive cells working in parallel.

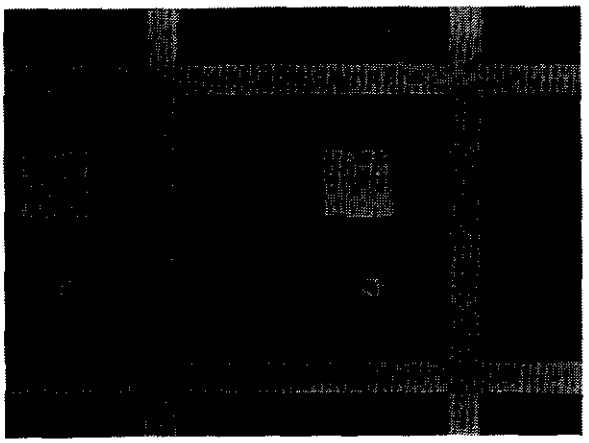

Fig. 4. Back side of CMUT chip: contact pad with via, solder bump pad and test pad.

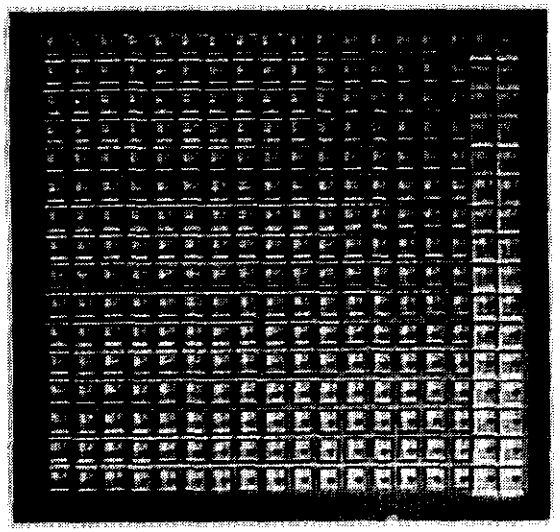

Fig. 5. Top view of a 16 x 16 element 2-D test array.

III. Experimental Characterization

A. Electrical characteristics of through wafer interconnect

The electrical characteristics of the through wafer interconnect are measured on several wafers with test structures. Resistivity measurements are performed on two conductive vias which are also connected as one big polysilicon pad on the front side. These measurements indicate a series resistance of 7Ω per via with less than 0.1Ω variation over the 16x16 element 2-D array. Given the fact that impedance of cMUT array element is in the kΩ range, this resistance should have a negligible effect on the array performance.

The cylindrical via and the top and bottom polysilicon islands form a capacitor to the bulk semiconductor substrate, which limits the high-frequency signal that is effectively transmitted through the via. Similarly, there can be significant crosstalk between vias through this capacitive path. One way to reduce the via capacitance, besides keeping the via diameter small, is to deplete the silicon bulk by applying a reverse bias to the diode formed by the n-type via conductor and the p-type silicon bulk (PN). This is especially convenient for cMUT arrays, since one should apply a DC bias for proper operation. Since the depletion region depth depends on the applied bias and the doping density, one can generate curves of capacitance as a function of these variables. A metal-insulator-semiconductor (MIS) structure can be formed in the via if the an oxidation is done after the via etch and before the polysilicon deposition. This structure does not have any DC leakage current, but it results in higher capacitances as compared to the PN structure for reasonable oxide layer thickness. Both these structures are fabricated and tested on wafers with different resistivity (doping density) and through via diameter. Figure 6 shows the results of these measurements. As expected, the PN structure can be driven into deep depletion when the junction is reverse biased. Hence, the via capacitance can be as low as 2 pF for a 100 μm diameter via on a wafer with 1000 Ω-cm resistivity. We have also fabricated 50 μm diameter vias and obtained 9 pF via capacitance on a wafer with 10 Ω-cm resistivity. This shows the potential of sub-pF via capacitance with a larger resistivity substrate (1000 Ω-cm or more). The measurement on the MIS structure with 1 μm oxide indicates that the capacitance reaches a minimum after inversion, which happens after 5 volts of reverse bias. These results are all in agreement with the predictions of simple semiconductor device theory.

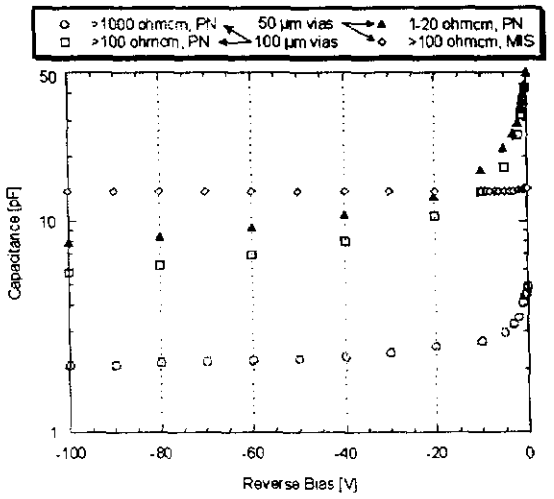

Fig. 6. Measured via interconnect capacitance.

B. Acoustic performance of array elements

The acoustic performance of 2-D cMUT array elements in transmission and reception is tested in oil. The details of this characterization can be found elsewhere [5]. The upper plot in Figure 7 shows the signal received by the cMUT element while a Panametrics V109 transducer 10 cm away is used as a transmitter and excited by a short DC pulse.

The frequency spectrum of the received signal is also plotted in the same figure. This single shot impulse response shows that the cMUT element has a 100% fractional bandwidth with some cross-coupling effects around 1 MHz. The through wafer interconnect does not introduce any adverse effect in acoustic performance of the transducer.

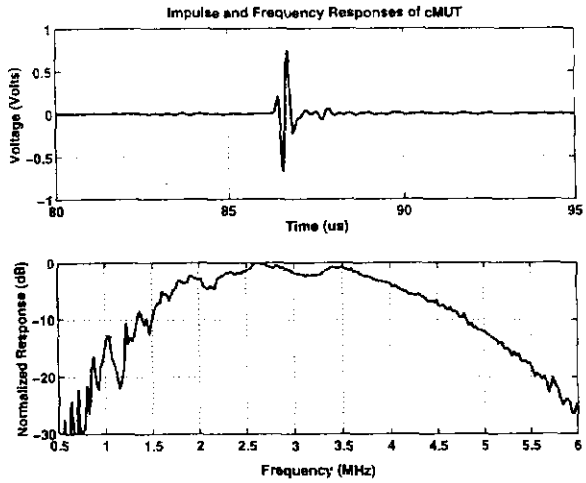

Fig. 7. Impulse response of a backside contacted 2-D array element.

IV. Conclusion

Highly integrated 2-D micromachined capacitive ultrasonic transducer arrays have been fabricated and tested. The transducer array includes individually addressable through-wafer interconnects ready for flip chip bonding to an electronic circuit die underneath the device. The interconnect resistance and capacitance are at suitable levels for ultrasound imaging with cMUTs. Acoustic performance of the array elements is also promising with wide bandwidth characteristics and no significant acoustic or electronic cross-coupling.

Acknowledgment

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