Controlled Two-Step Solid-Phase Crystallization for High-Performance Polysilicon TFT's

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***Abstract*— Solid-phase crystallization for polysilicon thin-film transistors (TFT's) is generally limited by a tradeoff between throughput and device performance. Larger grains require lower crystallization temperatures, and hence, longer crystallization times. In this letter, a novel crystallization technique is presented which increases both throughput and device performance, using a two-step process, controlled using an *in situ* acoustic temperature/crystallinity sensor. A high-temperature rapid thermal annealing (RTA) nucleation step is followed by a low-temperature grain growth step to grow large-grain polysilicon. TFT's have been fabricated with a substantial improvement in throughput and device performance. This promises a high-throughput, high-performance, spatially uniform TFT process.**

I. Introduction

POLYSILICON thin-film transistors (TFT's) are used increasingly in flat-panel display [1] and SRAM [2] applications. The channel films for these devices are typically deposited in the amorphous phase and crystallized to obtain smooth, large grain polysilicon [3]. Solid-phase crystallization (SPC) is a promising technique [4] due to its simplicity, low cost, and excellent uniformity. Unfortunately, SPC using low-temperature furnace annealing requires very long anneal times and hence suffers from a substantial tradeoff between performance and throughput. Rapid thermal annealing (RTA), while having high throughput [5], has poorer performance than low-temperature crystallization. Thus, the need exists for a means of improving the throughput of solid-phase crystallized TFT processes without sacrificing performance. A novel solution to this problem is detailed in this work, exhibiting improvements in both throughput and performance.

A method for temperature measurement using an acoustic sensor has been described previously [6]. An extension of the applications of this sensor to crystallinity tracking has also been described [7]. In this paper, the use of this sensor for *in situ* detection and control of temperature and crystallinity during two-step SPC is described. Films were crystallized using a combination of RTA and furnace annealing to achieve a substantial reduction in crystallization time. TFT's were fabricated and found to exhibit enhanced performance when compared to devices fabricated using standard single-step low-temperature SPC. This performance enhancement was accompanied by a substantial increase in process throughput.

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II. Background

A. Solid-Phase Crystallization

The crystallization from an amorphous phase to a (poly)-crystalline phase occurs through two processes—nucleation and grain growth [8]. Both have characteristic activation energies. The nucleation activation energy is extracted from the time to onset of crystallization, i.e., the incubation time, while the grain growth rate is extracted from grain progression data. For the SPC Si system, the nucleation activation energy is larger than the grain growth activation energy [9]. To achieve the largest possible grains, it is desirable to suppress nucleation relative to grain growth. Therefore, SPC is typically done at a low temperature. Unfortunately, this results in a reduction in throughput through an increase in the incubation time and a decrease in the grain growth rate. Higher temperatures increase throughput. However, excessive nucleation results in smaller grains and hence poorer performance.

RTA is considered a promising means of SPC. Recent advances in processing materials and technologies, such as the development of scanned RTA systems [10], have led to substantial progress in the development of RTA-based TFT technologies. The use of transient heating techniques, coupled with the poor thermal conductivity of glass enables the generation of a temperature gradient between the film and the glass, extending the glass-compatible temperature window [11]. Unfortunately, the higher temperatures result in smaller grain sizes. Therefore, a method for reducing the incubation time without sacrificing grain growth thermodynamic conditions is highly desirable.

Multistep annealing is well suited to the above requirement [12]. A short high-temperature step is used to nucleate the film, followed by a low-temperature step to maximize grain size. The ability to detect nucleation as a signal to initiate the quench is critical. The suitability of an acoustic sensor to this role has been demonstrated [7].

B. Acoustic Temperature/Crystallinity Sensor

An acoustic sensor to measure temperature has been developed previously [6]. PZT transducers bonded to quartz pins are used to pulse ultrasonic Lamb waves through the sample. The measured delay exhibits a linear variation with temperature. Therefore, it is possible to determine temperature from the time of flight of the acoustic waves through the wafer. This temperature measurement is independent of surface emissivity, etc., unlike other temperature measurement techniques

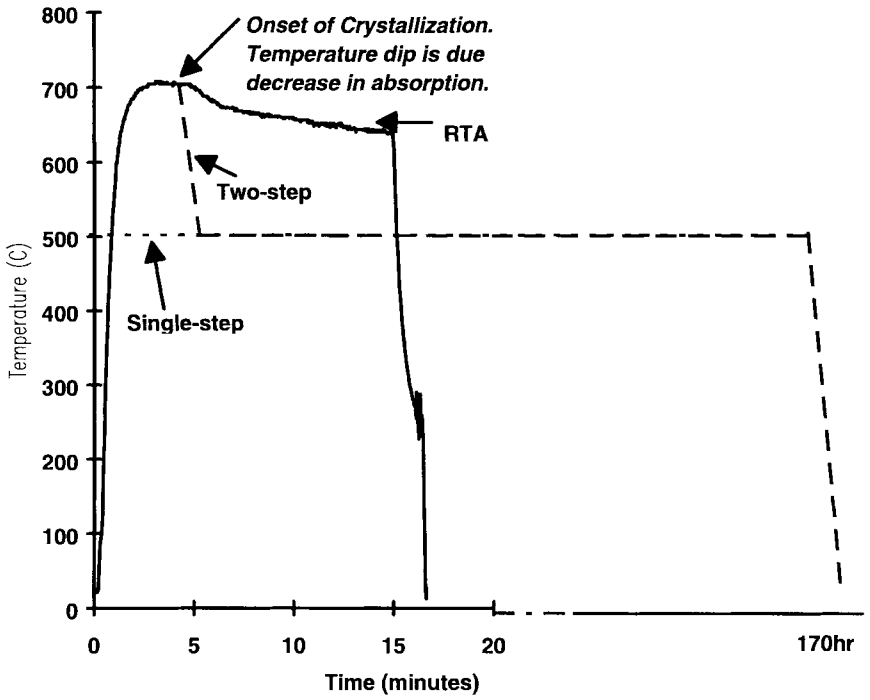


Fig. 1. Thermal cycles used during various crystallization anneals.

TABLE I
SUMMARY OF DEVICE CHARACTERISTICS

Process	Crystallization Time	Grain Size	Device Performance (W/L=20μm/20μm)							
			PMOS				*NMOS*			
			μ_{FE} ($cm^2/V{\cdot}s$)	sts (V/dec)	V_T (V)	I_{min} (pA/μm)	μ_{FE} ($cm^2/V{\cdot}s$)	sts (V/dec)	V_T (V)	I_{min} (pA/μm)
RTA	15min	3500Å	18	1.8	-12.4	1.1	27	0.92	5	0.47
1-step SPC	<168hr	4200Å	21	2.3	-9.9	6.1	34	0.69	5.6	0.24
2-step SPC	<24hr	5000Å	28	1.4	-8.9	1.5	41	0.56	5.7	0.27

μ_{FE} is defined at $|V_{DS}|$=0.1V, $|V_{GS}|$<30V

V_T is defined at $|V_{DS}|$=10V, $|I_D|$=100nA

Grain size is calculated from TEM by averaging the areas of 100 grains and determining the diameter of a circle of equal area.

such as pyrometry, and is thus well suited to crystallization processes on insulating substrates, where surface conditions change rapidly during the actual crystallization. It is possible to precisely and accurately measure the temperature of the substrate during annealing.

The optical absorption coefficient of an amorphous silicon film is reduced as it crystallizes. In the RTA of transparent substrates, this results in a reduction in the heat absorption by the sample, and hence in a drop in the substrate temperature. This phenomenon has been used to extend the acoustic sensor to crystallinity tracking. It has been determined that the sensor is sensitive enough to detect the onset of crystallization before any peaks are visible on X-ray diffraction spectra. This enables the use of the output of the acoustic sensor as an indicator for multistep annealing.

III. EXPERIMENTAL

1000 Å α–Si was deposited on fused silica wafers by LPCVD at 550 °C/500 mtorr from SiH_4. The wafers were annealed in the Stanford Rapid Thermal Multiprocessor [13]. An acoustic sensor was used for temperature/crystallinity tracking. The samples were heated to a substrate temperature of 700 °C using tungsten halogen lamps. Upon nucleation, the lamps were turned off and the wafers were placed into a furnace at 500 °C for complete crystallization. Control samples were also processed. These were either completely crystallized in the RTA or in the furnace. During the furnace anneals, the extent of crystallization was checked every 24 h. All crystallization was performed in an argon ambient. The thermal cycle processes are illustrated in Fig. 1.

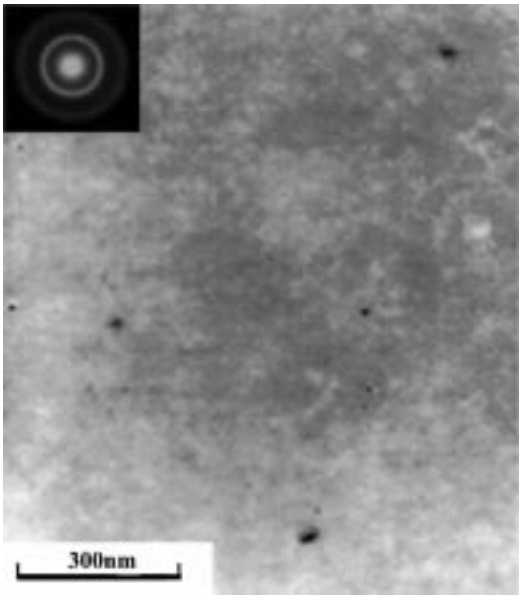


Fig. 2. Plan-view TEM at start of temperature quench in two-step process.

Upon crystallization, the films were patterned and TFT's were fabricated by a $\leq$600 °C planar top-gate self-aligned process using an LPCVD SiO_2 gate dielectric, ion implantation and furnace-based dopant activation, and plasma hydrogenation. Electrical measurements were made. Plan-view TEM's and selective area diffraction (SAD) measurements were also made at various stages throughout the crystallization process.

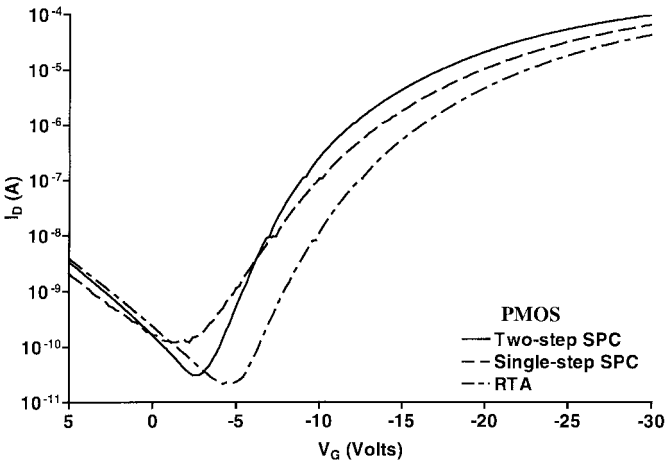
IV. Results

Fig. 2 shows the film at the point of quench as determined by the acoustic sensor. Clearly, the film is at the onset of crystallization. A few small crystallites (black in Fig. 2) are present in a sea of amorphous material. These act as growth-initiation centers during the low-temperature anneal. Quenching to a low temperature retards further nucleation, and hence, post-SPC grain size is larger than that for a single-step SPC film, which undergoes uniform homogeneous nucleation. Average grain size measurement from plan-view TEM indicates an increase on grain size of approximately 15%. This is accompanied by a seven-fold reduction in crystallization time. For comparison, films crystallized using RTA alone were also analyzed. The grain size is less than that for both one-step and two-step furnace annealed films.

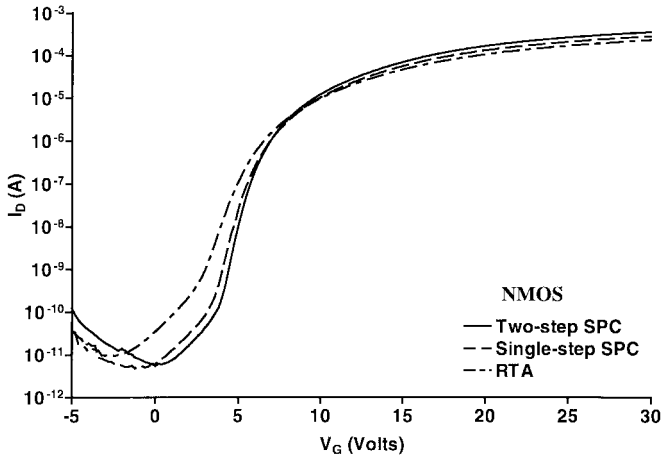
Electrical characteristics for PMOS and NMOS TFT's are shown in Fig. 3. Devices fabricated using two-step crystallization are superior to one-step furnace crystallized TFT's. Both of these exhibit better performance than TFT's fabricated using RTA crystallization, as is expected from thermodynamic considerations. Parameters for the various devices are summarized in Table I. In all cases, performance is best for devices fabricated using the two-step crystallization process.

V. Conclusions

An *in situ* controlled two-step crystallization process has been used in the fabrication of TFT's. A substantial improvement in throughput and device performance has been achieved. Process optimization should enable greater improvements. Fast, high-temperature nucleation should reduce substrate heating during RTA by increasing the temperature gradient across the glass. This should allow the use of cheaper low-temperature glasses to obtain a high-throughput, uniform polysilicon TFT technology.



(a)



(b)

Fig. 3. Electrical transfer characteristics for (a) PMOS and (b) NMOS TFT's.

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