Fabrication of CMUTs with Substrate-embedded Springs

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Abstract—A capacitive micromachined ultrasonic transducer (CMUT) with substrate-embedded springs, called post-CMUT (PCMUT), decouples the spring constant and the mass of the system by realizing the former using relatively long and narrow posts. The PCMUT improves on the fill factor and average volume displacement of the conventional CMUT as shown in our previous work using 3-D finite element analysis (FEA). This work reports on second-generation PCMUT devices designed according to our 3-D FEA simulation results and manufactured using an improved fabrication process flow. This improved fabrication process is composed of three critical steps: wafer bonding of two silicon-on-insulator (SOI) wafers, deep reactive-ion etching (DRIE) of posts (i.e. springs), and precision wafer polishing. The improved fabrication process results in a flexible platform for 82-element 1-D arrays, a single element device for high-intensity focused ultrasound (HIFU), and test PCMUT element structures. The new fabrication process also provides better post high uniformity as well as a clear path toward making 2-D arrays.

Keywords—Ultrasound; CMUT; PCMUT; substrate-embedded springs; MEMS; FEA

I. INTRODUCTION

A capacitive micromachined ultrasonic transducer (CMUT) with substrate-embedded springs, called post-CMUT (PCMUT), decouples the spring constant and the mass of the system by realizing the former using relatively long and narrow posts and the latter by a stiff plate residing on the posts[1]. The PCMUT structure improves on the fill factor and average volume displacement of the conventional CMUT structure as shown in our previous work using 3-D finite element analysis (FEA) [2]. As shown in Fig. 1(a) and 1(b), we have previously demonstrated the functionality of the PCMUT using a simple fabrication process [1]. However, this process suffered from several issues including post height nonuniformity (Fig. 1(c)) and asymmetric response due to the front-side electrical connection [Fig. 1(d), (e)]. Our simple first-generation PCMUT fabrication process did not yield uniform post height due to nonuniform deep reactive-ion etching (DRIE) through different pattern sizes nor offered a clear path toward making 2-D arrays due to the complicated front-side electrical connection.

In this work, we report on second-generation PCMUT devices designed according to our 3-D FEA simulation results and manufactured using an improved fabrication process flow. This improved fabrication process is composed of three critical steps: wafer bonding of two silicon-on-insulator (SOI) wafers, DRIE of posts (i.e. springs), and precision wafer polishing. The improved fabrication process results in a flexible platform for 82-element 1-D arrays, a single element device for high-intensity focused ultrasound (HIFU), and test PCMUT element structures. The new fabrication process also provides better post high uniformity as well as a clear path toward making 2-D arrays.

Fig. 1. (a) Cross-sectional schematic of 1st-generation PCMUT. (b) Cross-sectional SEM image of 1st-generation PCMUT. (c) SEM image of silicon posts. (d) 3-D perspective view of 1st-generation PCMUT. (e) Asymmetric modal response of 1st-generation PCMUT.
II. Method

A. PCMUT Device Structure

We have previously reported on the PCMUT functionality as well as the parametric study of the structure [2]. For this work, we started with the same design parameters of the previous study and modified some of them such as the effective gap height. Since in practice several hundreds of nanometer thick silicon dioxide layer exist between the two electrodes for the purpose of electrical isolation in the case of contact, the effective gap height is increased from 150 nm to 250 nm. Fig. 2 and Table I show the design parameters of one PCMUT cell. We targeted this 2-D PCMUT element with a center frequency of about 4 MHz. Also a one-way -3-dB fractional bandwidth of about 100% was considered as a design target for the medical ultrasound imaging.

Fig. 2. A cross-sectional drawing of a PCMUT cell.

<table>
<thead>
<tr>
<th>TABLE I. DEVICE PARAMETERS</th>
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<tr>
<td>Post Diameter (d_post)</td>
</tr>
<tr>
<td>5 μm</td>
</tr>
<tr>
<td>Plate 1 Width (W_plate1)</td>
</tr>
<tr>
<td>120μm</td>
</tr>
<tr>
<td>Plate 2 Width (W_plate2)</td>
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<td>100μm</td>
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Fig. 3 shows a 3-D perspective drawing of a single PCMUT element. The element consists of four cells. The piston top plate provides nonflexural plate movement, which resembles the ideal piston movement [3]. In order to eliminate the asymmetric response due to the front-side electrical connection, as shown in Fig. 1(d), we use a continuous highly-doped silicon plate 1 or a thin top plate as a common electrode. By replacing a bulk substrate wafer with an SOI wafer, we can embed the signal electrode into the substrate to connect the four cells and sustain the mechanical symmetry. The frame electrode is formed around the PCMUT element. It is connected to the ground to improve noise immunity and reduce electrical crosstalk.

Fig. 3. 3-D perspective drawing of a single PCMUT element.

B. Finite Element Analyses

We developed a 3-D FEA model for transient analysis using ANSYS (ANSYS, Inc., Canonsburg, PA) in order to estimate average surface acoustic pressure and its frequency spectrum for our device. We also performed harmonic analysis to compare the frequency spectrum with the result of the transient analysis. We biased the PCMUT element at 129.1 V, which is 80% of the simulated pull-in voltage. We applied a 200-nsec bipolar 70-Vp-p pulse for the transient analysis. The corresponding simulated average surface acoustic pressure is shown in Fig. 4. The transient simulation data shows a peak-to-peak average pressure of 1.8 Mpa at the face of the transducer [Fig. 4(a)]. The corresponding frequency spectrum is shown in

Figure 4. 3-D FEA simulation results of average surface acoustic pressure: (a) transient response, and (b) frequency spectra.
solid blue line in Fig. 3(b). A -3-dB fractional bandwidth of 84.7% around the center frequency of 4 MHz can be obtained from the transient analysis. Compared to the result of the harmonic analysis, our transient analysis model not only shows consistent agreement but also gives an indirect evidence that the unrealistically exaggerated mutual interaction among 4 cells, which shows up as a sharp dip in the harmonic analysis result shown in dashed line in Fig. 3(b).

C. Fabrication Process

The proposed fabrication process is composed of three critical steps: wafer bonding of two SOI wafers, DRIE of posts (i.e. springs), and precision wafer polishing. Combining the wafer bonding process of two SOI wafers and DRIE process leads to a more uniform post height. Also, combining the wafer bonding and wafer polishing can provide a uniform piston top plate as well as the thin top plate.

The process starts with an SOI substrate wafer having a device layer of 50 μm. This device layer height determines silicon post height. This wafer is oxidized and patterned to define lateral dimension of the PCMUT cavities [Fig. 5(a)]. Then, the wafer goes through a second thermal oxidation that defines the cavity height or the effective gap height [Fig. 5(b)]. Shallow trenches are etched into the device layer using an RIE process in order to maintain the electrical connections between multiple cells corresponding to an element [Fig. 5(c)]. This step also ensures device’s mechanical symmetry in order to avoid undesired operation modes.

Next, silicon posts and bottom electrode isolation pattern are defined using a DRIE process by etching through the 50-μm device layer [Fig. 5(d)]. Particular attention should be given to this step since the diameter of posts are one of the most important components for the performance of a PCMUT. After a short oxidation to passivate the exposed sidewalls [Fig. 5(e)], another SOI wafer is bonded to the substrate SOI wafer using a fusion bonding process under vacuum [4][5]. Device layer properties of this new SOI wafer determine conductivity, thickness and uniformity of the thin top plate. The handle of the bonded SOI wafer is then polished to a final thickness of 20±1 μm to create the stiff section of the PCMUT top plate [Fig. 5(f)].

The remaining 20-μm handle layer and the box layer of the top SOI wafer is patterned and etched to define the piston top plate [Fig. 5(g)]. The 250-nm thick device layer of this SOI wafer constitutes the edge section of the top plate. This edge section is necessary to hold the vacuum condition inside the cavities. Finally, the electrical connections to top and bottom electrodes are created using silicon and oxide etching and aluminum deposition and patterning steps [Fig. 5(h)].

III. RESULTS AND DISCUSSION

Fig. 6(a) shows the SEM image of a fabricated single PCMUT cell where the piston and thin top plate were intentionally removed. Another piston top plate can be clearly seen behind the stripped PCMUT cell. The place where nine posts were located is exposed from the top plate removal. Fig. 6(b) shows the SEM image of the nine silicon post springs attached on the top SOI wafer. The SEM image infers that the bonding strength of the interface between the top SOI wafer and the silicon post springs is strong enough so that the...
detachment occurs on the interface between the BOX layer and the device layer of the bottom SOI substrate. A single test PCMUT element with the three aluminum electrodes is shown in Fig. 6(c). An 82-element 1-D PCMUT array measuring 24 mm by 15 mm die size was fabricated with the new process as shown in Fig. 6(d). Fig. 5(e) shows a single-element PCMUT with 1185 cells for HIFU applications.

An exemplary measurement result, obtained from a single test PCMUT element, demonstrates strong acoustic response in the electrical input impedance in air (Fig. 7). Simulating the exact structure based on the dimensions achieved in the fabrication proves good agreement between the measurement and the simulations, which predicted a resonant frequency of 3.3 MHz in air.

In particular for large arrays such as a 1-D PCMUT array and a single element PCMUT, the vacuum cavities are all connected due to the electrical connections. In addition, large area is sealed by the fragile 250-nm thin top plate. This poses a great challenge for getting good yield for those devices. We are currently working on improving the electrical connectivity by backside electrical access.

IV. CONCLUSIONS

We have developed an improved PCMUT fabrication process that, among other benefits, provides better post height uniformity. Because of the wafer bonding of two SOI wafers, the buried silicon dioxide layer provides an etch stop leading to a uniform post height. Additionally, by combining with the DRIE process, more design flexibility for the electrical connection of PCMUT can be achieved. From this improvement, we can demonstrate versatile devices such as 82-element 1-D arrays, a single element device for HIFU, and test PCMUT element structures. Furthermore, with some modifications, this process can be adopted for 2-D arrays with backside electrical access.

ACKNOWLEDGMENT

This work was supported by the National Institutes of Health (NIH) under grant 5R01HL67647 and 5R01CA134720 and Analog Devices. We fabricated the PCMUT devices at the Stanford Nanofabrication Facility (Stanford, CA), a member of National Nanotechnology Infrastructure Network. We would like to thank Timothy Brand for help with grinding and polishing processes. We would also like to thank Dr. Sangmoo Jeong for help with SEM pictures.

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