Fabrication of Capacitive Micromachined Ultrasonic Transducers via Local Oxidation and Direct Wafer Bonding

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***Abstract*—We present the successful fabrication of capacitive micromachined ultrasonic transducers (CMUTs) with an improved insulation layer structure. The goal is to improve device reliability (electrical breakdown) and device performance (reduced parasitic capacitance). The fabrication is based on consecutive thermal oxidation steps, on local oxidation of silicon (LOCOS), and on direct wafer bonding. No chemical-mechanical polishing step is required during the device fabrication. Aside from the advantages associated with direct wafer bonding for CMUT fabrication (simple fabrication, cell shape flexibility, wide gap height range, good uniformity, well-known material properties of single-crystal materials, and low intrinsic stress), the main vertical dimension (electrode separation) is determined by thermal oxidation only, which provides excellent vertical tolerance control ($<$10 nm) and unprecedented uniformity across the wafer. Thus, we successfully fabricated CMUTs with gap heights as small as 40 nm with a uniformity of $\pm$2 nm over the entire wafer. This paper demonstrates that reliable parallel-plate electrostatic actuators and sensors with gap heights in the tens of nanometer range can be realized via consecutive thermal oxidation steps, LOCOS, and direct wafer bonding without chemical-mechanical polishing steps. [2010-0197]**

***Index Terms*—Capacitive micromachined ultrasonic transducer (CMUT), direct wafer bonding, electrical breakdown, local oxidation of silicon (LOCOS), parasitic capacitance, patterning of silicon via oxidation.**

I. Introduction

MINIATURIZED MEMS-based acoustic transducers, suitable for generating and detecting sound waves, have been widely researched as alternatives for macroscale devices. Examples include MEMS-based microphones and speakers [2], [3], which offer advantages such as low cost, low power consumption, and small footprint. Our focus is on miniaturized MEMS-based acoustic transducers that utilize the electrostatic force between two electrodes, connected to an electrical voltage source. Usually, these electrodes, of which one can vibrate to generate or receive ultrasound, are arranged in a parallel-plate capacitor configuration [4], [5]. In the meantime, the established term for these transducers is capacitive micromachined ultrasonic transducers (CMUTs), because the complete transducer is micromachined, i.e., including the vibrating part. This is not the case for the more general and far longer existing type of condenser transmitters and microphones for airborne ultrasound [6] or later realizations, such as described for example in [7].

Today, available MEMS technologies allow fabricating CMUTs for a wide range of frequencies, ranging from several kilohertz up to more than hundred megahertz. This flexibility helps to provide a powerful technology platform for various applications that can benefit from these MEMS-based acoustic transducers. Examples are larger transducers for airborne applications that operate around 50 kHz [8]; transducer arrays operating in immersion around 2.5 MHz for therapeutic applications such as high-intensity focused ultrasound [9]; transducers operating in immersion at higher frequencies [10]; and transducers operating in air at frequencies up to 42 MHz for chemical/biosensor applications [11].

Some of the reasons why the CMUT technology is so versatile include the following: The fabrication of the complete transducer including the vibrating part (plate[1]) allows a rugged design due to the permanent attachment of this plate to the substrate; the transducer can have a vacuum gap that improves transduction efficiency (no squeeze film damping) and reliability in terms of electrical breakdown in the area where the plate is free to move; depending on the fabrication method and materials used, an excellent prediction of the transducer characteristics is possible; and due to the low mechanical impedance of the thin and lightweight plates, CMUTs have an inherent advantage over piezoelectric transducers for airborne ultrasound applications and do also feature a large acoustic bandwidth easily exceeding 100% in immersion.

The basic operation principle can be understood by looking at Fig. 1(a), which shows a cross section of a single-cell of the CMUT fabricated using a sacrificial release process [12]. In principle, the CMUT features a parallel-plate structure with

Manuscript received June 28, 2010; revised October 19, 2010; accepted November 2, 2010. Date of publication January 10, 2011; date of current version February 2, 2011. This work was supported by the Defense Advanced Research Projects Agency under Grant N66001-06-1-2030. Subject Editor H. Zappe.

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Digital Object Identifier 10.1109/JMEMS.2010.2093567

[1]In the literature, the term membrane is often used for the moving part of the CMUT cell. In the proper meaning of the word, a membrane, however, has per-definition zero resistance against bending forces (out-of-plane stress). Thus, in this paper, we will use the correct term *plate*, because the CMUT described in this paper, as almost every CMUT [18], operates in a pure plate regime (deflection-to-thickness ratio smaller than 10%) dominated by out-of-plane stress (bending stress).

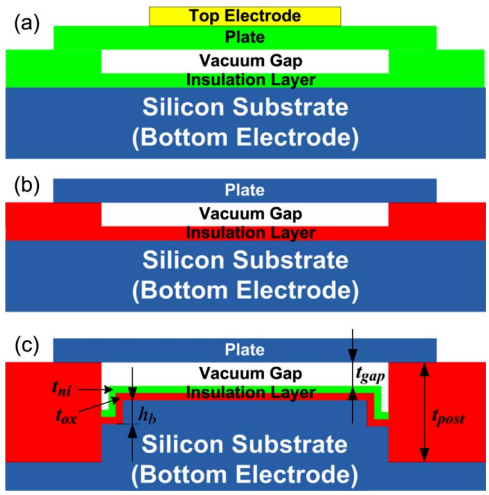

Fig. 1. Cross-sectional schematic of a CMUT based on (a) sacrificial nitride process, (b) conventional wafer bonding process, and (c) LOCOS/wafer-bonding process demonstrated in this paper.

two electrodes. By applying an ac or transient signal to these electrodes, an electrostatic force occurs that acts on the top electrode. This top electrode can be attached to an electrically insulating transducer plate [Fig. 1(a)] or the transducer plate itself can be electrically conductive and act as the top electrode as shown in Fig. 1(b). By superimposing the ac signal on top of a larger dc voltage, the transducer's sensitivity is increased tremendously, and the transducer is biased in a more linear voltage-to-force regime.

In a sacrificial release layer process [12], which is based on thin-film deposition and etching steps, the plate material (e.g., silicon nitride) is deposited on a patterned sacrificial thin film (e.g., polysilicon). Then, this sacrificial layer is etched, which releases the plate by forming a cavity beneath. For a vacuum-sealed device [Fig. 1(a)], a low-pressure chemical vapor deposition (LPCVD) step is used to vacuum seal the cavity. Because thin-film deposition steps dominate this fabrication process, the device characteristics are difficult to predict. Known issues are nonuniformities, reduced effective gap heights due to surface roughness [13], in-cavity deposition during the sealing step [14], intrinsic stress inside the plates [15], and thermal-stress effects between the electrode and plate material [16].

All of these issues can be addressed by avoiding thin-film deposition steps for the key components of a CMUT cell. This was demonstrated in [17] by fabricating CMUTS via direct wafer bonding. The cavity is formed by thermal oxidation and patterning this oxide layer, then a silicon-on-insulator (SOI) wafer is bonded to the substrate with the goal to transfer the active layer to the substrate wafer [Fig. 1(b)]. After removing the carrier wafer and buried oxide (BOX) layer, the remaining silicon plate can be patterned to define the transducer. Such direct wafer-bonded devices show excellent uniformity and predictability in terms of various characteristics such as static plate deflection, dynamic plate displacement, resonance frequency, quality factor, and pull-in voltage. SOI wafers are available off the shelf with excellent quality (surface smoothness, total thickness variation of the active layer, and crystal orientation), and silicon is one of the best-characterized materials in terms of its mechanical and electrical properties.

As proposed in [19], a cell structure as shown in Fig. 1(c) that has an electrically conductive plate and a vacuum gap can be significantly improved in terms of reliability (electrical breakdown) and performance (higher coupling efficiency due to reduced parasitic capacitance) by using an extended insulation layer structure, i.e., by extending the silicon dioxide layer into the substrate [see Fig. 1(b) in [19]]. Note that, in the conventionally fabricated wafer-bonded CMUT cell [Fig. 1(b)], the insulation layer thickness at the bottom of the cavity and the oxide thickness at the area surrounding the cavity (nonactive area or oxide post area) are inherently linked to each other. The desire to realize CMUTs with small electrode separations (gap heights) and, thus, low dc-voltage requirements would lead to designs with thin oxide post thicknesses, which translate into larger parasitic capacitance values and lower electrical breakdown voltages.

The goal of this paper, which is an extended version of our conference paper [1], is twofold. First, we introduce a fabrication process based on LOCOS and direct wafer bonding that allows the precise fabrication of the beneficial CMUT cell structure as shown in Fig. 1(c), which features the extended insulation layer structure as proposed in [19]. Second, we demonstrate that direct wafer bonding is possible after LOCOS without chemical-mechanical polishing, assuming that certain thickness limits of the grown silicon dioxide are not exceeded.

In the following sections, we first present the fabrication process in detail and provide key design guidelines of a CMUT fabricated via LOCOS and direct wafer bonding. Then, we present fabrication and measurement results of the fabricated device before we discuss the results in detail.

II. Method

A. Fabrication Process Description

As shown in Fig. 1(c), our goal is to fabricate a CMUT cell structure with a small gap height and a thick insulation layer thickness (silicon dioxide) in the postregion. We start with patterning the silicon substrate first to generate a silicon bump, which facilitates the realization of such a large ratio of gap height to oxide post thickness. Our target gap height is only 40 nm for this device, which requires excellent vertical dimension control over the entire wafer. Thus, instead of etching, the silicon substrate by conventional plasma etching, or wet etching techniques, we use two consecutive thermal oxidation steps. After oxidizing the substrate, we pattern the oxide by standard lithography and etching [Fig. 2(a)]. In the second oxidation step, the exposed silicon area (this will become the postarea) oxidizes faster due to the slower oxygen diffusion rate in the already oxidized regions. The result is a silicon-to-oxide surface profile as shown in Fig. 2(b). After removing the oxide, the substrate features the required pattern of precise height and shape [Fig. 2(c)].

Now, the substrate is prepared for the next fabrication steps, but first, we will define two distinguished regions: the protruding silicon bumps, which will become the bottom electrodes in each cell, and the remaining area, which will be used for forming the oxide post (extended insulation layer). We have

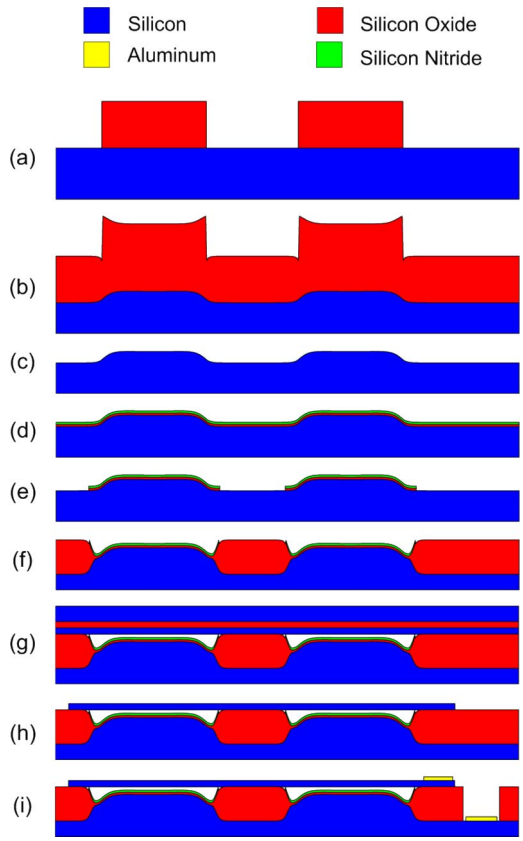

Fig. 2. Schematic view of the fabrication flow proposed in this paper. (a) Thermal oxidation followed by oxide patterning. (b) Thermal oxidation. (c) Etching grown oxide by 6:1 BOE. (d) Thermal oxidation followed by silicon nitride (Si_3N_4) deposition by LPCVD. (e) Patterning of the ON layer by plasma etching and wet etching (20:1 BOE). (f) Local oxidation. (g) Direct wafer bonding of SOI wafer and annealing. (h) Removing the carrier wafer and BOX layer followed by the patterning of the silicon plate. (i) Patterning the silicon oxide followed by the deposition and patterning of the aluminum.

identified the classical[2] local oxidation of silicon (LOCOS) technique as an optimum solution to fabricate such an extended insulation layer, i.e., the oxide posts. This idea supports all key requirements. First, the top surface of the oxide posts can be made higher than the protruding silicon bumps in order to form cavities. Second, a tight vertical-dimension control with good uniformity over the entire wafer is possible, i.e., a precise gap height control. Third, the oxide posts grow into the substrate as well, which results in thicker oxide posts. As mentioned before, this is preferred in order to reduce the parasitic capacitance and to increase the electrical breakdown voltage [19].

Thus, we continue with depositing an oxygen-blocking layer required for LOCOS. A thin stoichiometric silicon nitride layer on top of a thin thermal-grown oxide layer is a good choice. Then, this oxide–nitride (ON) layer [Fig. 2(d)] is patterned and etched to expose the silicon substrate for the actual LOCOS step [Fig. 2(e)]. The nitride layer is etched using plasma etching, and the oxide underneath acts as etch stop. The oxide layer beneath is easily removed by wet etching, which ensures good surface smoothness of the exposed silicon. Note that, in this process, this ON layer fulfills two purposes: first, it acts as an oxygen barrier during the LOCOS step, and second, it will be used as a thin insulation layer at the bottom of each cavity, as already shown in Fig. 1(c). The expected result after the LOCOS step is shown in Fig. 2(f).

The main question in this step is whether this wafer can be directly bonded to the SOI wafer as shown in Fig. 2(g). In general, as long as certain criteria are fulfilled, a successful direct wafer bonding can be expected. First, a low surface roughness value (lower than ~ 5 Å_{RMS}) is important. Second, a flat top surface (no protrusion) is required. Third, a sufficiently large bonding area providing enough surface energy [20] to overcome the tension in the wafers (curvature) is essential. In our process, the wafer at the stage, as shown in Fig. 2(f), fulfills all of these criteria, and compared to other wafer-bonded CMUTs, our extended insulation layer is directly grown out of the substrate. As a result, there are no fabrication process steps required between the LOCOS step and the wafer-bonding step, i.e., the wafers can be directly loaded from the oxidation furnace into the vacuum chamber of the wafer-bonding tool. This method prevents potential contaminations on the wafers during additional process steps, such as lithography, and does not require chemical-mechanical planarization before the bonding step.

After the direct bonding step and annealing at 1050 °C for increased bonding strength [Fig. 2(g)], the rest of the fabrication process is state of the art [17]. It consists of two parts. First, after removing the handle wafer, the silicon plate can be defined by standard lithography. Second, for electrical connection, the top and bottom bonding pads are fabricated. Due to the high doping concentration, the silicon plate acts as a top electrode and, thus, does not require any metallization. This has advantages in terms of improved cell-to-cell uniformity and zero thermal-induced stress effects due to thermal expansion coefficient mismatch between the silicon and the metal. Only in the case the device needs both connections on the front side, the thick oxide post must be opened for the ground pad connection. As a result, only four lithography masks (five masks, when substrate connection on the front side is required) have been used to fabricate the device as shown in Fig. 1(c).

B. Design Guideline

As mentioned previously, a large ratio between oxide post thickness and gap height is beneficial. For the device design, however, there are certain limitations that we need to consider to achieve both a successful device fabrication and functional operation. The key dimensions of a resonant structure are the radius and the thickness of the plate. In first order, for a given plate thickness, the radius of the plate follows from the specified resonant frequency. For example, with a 500-nm-thick silicon plate, vibrating in vacuum under zero bias voltage, a plate radius of 6 and 20 μm corresponds to the resonant frequencies of 53 and 4.8 MHz, respectively [11].

[2]Two consecutive oxidations in the previous paragraph are also similar to LOCOS process, because we use thick oxide to partially block oxygen. In this paper, we only use the term LOCOS when an oxygen-blocking layer such as a silicon nitride is used. As an alternative, the classical LOCOS process can replace two consecutive oxidations to fabricate the silicon bumps. However, because this would require additional process steps to remove the nitride layer, we propose to use the described method of two consecutive oxidation steps.

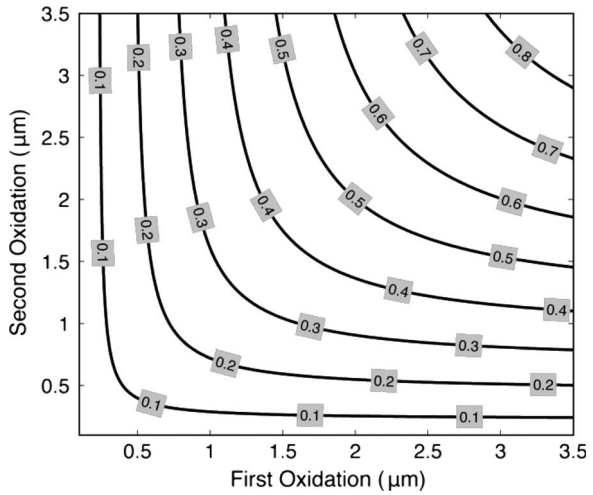

Fig. 3. Calculated height of the silicon bump [Fig. 2(d)] for different combinations of the first [Fig. 2(a)] and second oxidation [Fig. 2(c)] thicknesses.

In terms of the feasibility of the fabrication process, the radius of the silicon bump inside the cavity [Fig. 2(c)] must be smaller than the radius of the plate. The reason is evident in Fig. 2(f). We want the edge of the LOCOS mask to be located in the flat region of the silicon area as shown in Fig. 2(e). This ensures a flat top surface of the oxide post, which would not be the case, if the edge of the LOCOS mask is located on the silicon bump area. In the later case, the profile of the silicon bump would be transferred to the top surface of the grown oxide post. Based on our experience, we recommend that the size of the LOCOS mask to be larger than the silicon bump by about twice the thickness of the oxide post [Fig. 2(e)].

Again, the essential part of the process, proposed in this paper, is the fabrication of the large ratio between the gap height and the thickness of the oxide post. This large ratio is feasible because of two reasons: the silicon bump inside the cavity and the oxide post by LOCOS process [Fig. 1(c)]. As described in the previous section, the silicon bump height is a result of two consecutive oxidations. Its height can be calculated based on well-known thermal oxidation models such as by Deal–Grove [21], as shown in Fig. 3. However, because we use 6:1 BOE to remove the oxide in Fig. 2(c), there is an optimal combination of first and second oxidation thicknesses [Fig. 2(a) and (b)].

The oxide on the silicon bump will always be thicker than the oxide on the postregion. As a result, the silicon in the postregion will inevitably be exposed to the 6:1 BOE until the oxide on the silicon bump is removed as well. As Miki [21] investigated, a longer exposure time of silicon to BOE will gradually decrease the available surface energy. For example, after the 5 min exposure of silicon in 7:1 BOE, the available surface energy drops by 14% (from 70 to 60 mJ/m^2). However, five more minutes will give another drop of even 33% (from 60 to 40 mJ/m^2). For this reason, our approach is to keep the exposure time in 6:1 BOE as short as possible. This can be achieved by choosing the second oxidation thickness as large as possible. However, there is a limit for the second oxidation thickness because a too thick second oxidation tends to reduce the flat portion of the silicon bumps due to a more rounded shape.

The ON layer fulfills two purposes. It acts as an oxygen-blocking layer for the LOCOS step. In addition, it will serve as the insulation layer in the cavity of the device [Fig. 1(c)]. For the successful LOCOS step, the nitride layer (oxygen-blocking layer) should be thick enough and free of pinholes. As Mizuno demonstrated [23], a silicon nitride with a thickness of 52 nm successfully blocks oxygen during a 0.83-μm-thick LOCOS step. We select our thickness for the nitride in a similar thickness range for about 1-μm-thick LOCOS step. The oxide layer beneath the nitride layer has the sole purpose of acting as an etch stop for the plasma etching step [Fig. 2(e)] which determines its thickness.

For reliable operation in terms of electrical breakdown inside the cavity region, we design the thickness of the ON layer for the worst case. Because we have vacuum in the cavity, the worst case occurs when the plate contacts the ON layer (pull-in or too large plate movement). Based on these criteria, as stated earlier, we choose 60-nm-thick nitride and 30-nm-thick oxide for a $\sim 1-\mu$m-thick LOCOS step.

For the feasibility of the wafer bonding process, the wafer after performing the LOCOS step [Fig. 2(f)] should have minimal curvature. This can be achieved by removing the ON layer on the backside of the wafer before growing the thick oxide post [Fig. 2(e)]. As a result, we will have the same amount of oxide (compressive stress) on both sides, which ensures low curvature. The curvature of the wafer will depend on the total area of the postregion. By partially etching the oxide on the backside, this effect can be compensated.

The LOCOS step elevates the bonding surface to the target gap height. The gap height is estimated as

$$t_{\mathrm{gap}} = 0.56 t_{\mathrm{post}} - (h_b + t_{\mathrm{ox}} + t_{\mathrm{in}}) \tag{1}$$

where t_{gap}, t_{post}, t_{ox}, t_{ni}, and h_b are the thicknesses of the gap, the oxide post, the oxide insulation layer, the nitride insulation layer, and the height of the silicon bump, respectively [Fig. 1(c)]. In this device, it is essential to have a good controllability and uniformity of the gap height. The thickness of the ON layer $(t_{\mathrm{ox}} + t_{\mathrm{ni}})$ is small compared to the silicon bump height (h_b) and the oxide post thickness (t_{post}). Note that, in this fabrication process, these two dimensions are only determined by thermal oxidation. Therefore, this process inherently features a precise and uniform gap height control.

III. Result

A. Fabrication Result

During device fabrication, we monitored the vertical dimensions and the surface roughness to verify the feasibility of the fabrication process. After two consecutive oxidations of 2000 and 640 nm [Fig. 2(a) and (b)] and the subsequent removal of the oxide [Fig. 2(c)], the height of the silicon bump was measured to be 220 nm, as expected. The surface roughness of the bonding area in this step [Fig. 2(c)] was 2.24 $\mathrm{Å}_{\mathrm{RMS}}$, which is slightly increased, compared to the surface roughness of the bare silicon substrate used (1.8 $\mathrm{Å}_{\mathrm{RMS}}$).

As mentioned previously, the main step in this process is the LOCOS step [Fig. 2(f)]. An atomic force microscope (AFM)

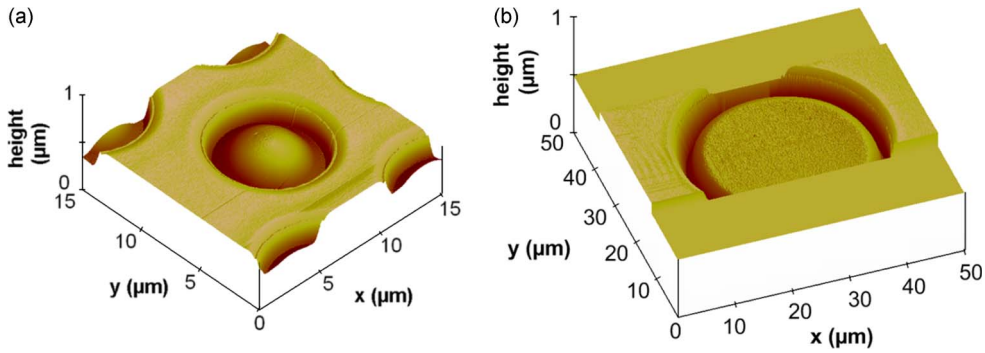

Fig. 4. AFM images of the cavity and the oxide post after the LOCOS process [Fig. 2(g)]. The measured step height between the oxide post and the silicon bump is (a) 39.8 and (b) 130 nm.

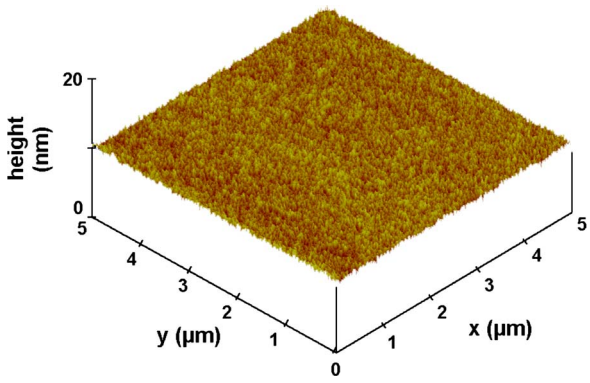

Fig. 5. AFM image of the flat area of the oxide post after the LOCOS process [Fig. 2(g)]. The measured surface roughness is 2.36 Å_{RMS}.

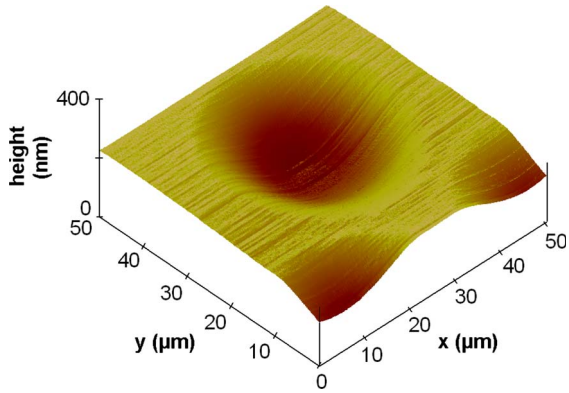

Fig. 6. AFM image of the silicon plate [Fig. 2(h)]. The static deflection due to atmospheric pressure proves that fusion bonding is successful because it maintains vacuum in the cavity beneath.

measurement after the LOCOS step provided both the profile of the structure (gap height) and the surface roughness of the bonding area. The profile measurement allowed confirming the four criteria. First, the gap height was 39.8 ± 2.5 nm across the entire wafer and 130 ± 3 nm on a second wafer containing a large gap design (Fig. 4). Second, the grown oxide (the post) was flat between the cavities (bonding area). Third, the edge of the LOCOS mask was lower than the height of the grown oxide. Last, the surface roughness of the oxide post in the bonding area was 2.36 Å_{RMS}, which was low enough for the direct bonding step (Fig. 5). Note that, in case the measured gap height is too low, one can continue the oxidation for a designed gap height.

The first verification of the successful direct wafer bonding to this LOCOS-grown structure was done by IR imaging after unloading from the vacuum-bonding tool. This allowed confirming a void-free bond over the entire area of the wafer before and after the annealing step [Fig. 2(g)]. The second verification of a good bonding quality was the fact that removing the handle wafer (grinding and wet etching by tetramethylammonium hydroxide, TMAH) and defining the elements (plasma etching) did not result in a reduction of the yield [Figs. 2(h) and 8]. Last, the most important verification was monitoring the static deflection of the plate, because only good bonding quality ensures good vacuum sealing of the cavity (Fig. 6). For the plate with a radius of 20 μm, we measured a static deflection of 122 nm, as expected.

After the fabrication of devices, the wafer was cleaved and inspected in an SEM to verify the cross-sectional profile

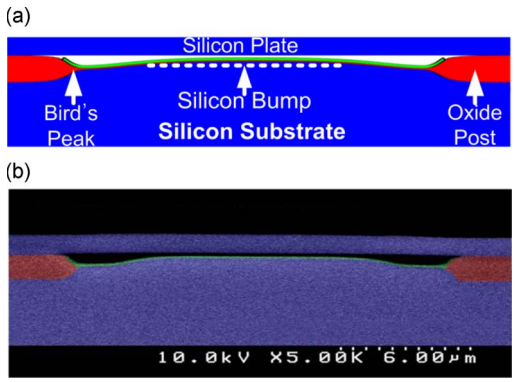

Fig. 7. Cross-sectional view of the CMUT cell by (a) TSUPREM simulation and (b) colored SEM of the fabricated device which has 130-nm gap. The color code is the same as in Fig. 2.

[Fig. 7(b)]. The measured cross section confirmed both the TSUPREM-4 (Synopsys, Inc., Mountain view, CA) simulation result [Fig. 7(a)] and the AFM measurement in terms of the flat silicon bump, the oxide posts with bird's peaks, and the target gap height.

The fabricated devices were inspected under the optical microscope (Fig. 8). The configuration of the prototype is a 1-D array. The die size of the prototype is 10 mm $\times$ 5 mm, where it contains 32 or 64 elements and the pitch is 300 μm. For our specific application (multiple plate resonator), through-wafer trenches were located between the elements in order to minimize the effect of the surface and bulk acoustic wave

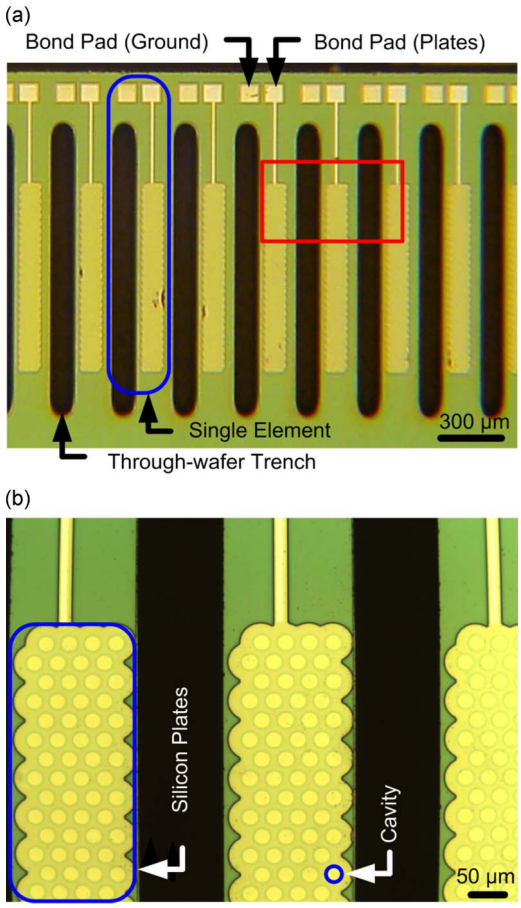

Fig. 8. Optical photographs of the fabricated CMUT. This particular device shown has a silicon plate with a thickness of 0.5 μm and a cavity radius of 9 μm. (a) Each element consists of 200 resonators (cells) and two bond pads to access the plate and the ground. Through-wafer trenches are located between the elements to reduce mechanical interference between the elements. (b) Zoomed-in picture of the red area in (a). The circular cavity is clearly visible.

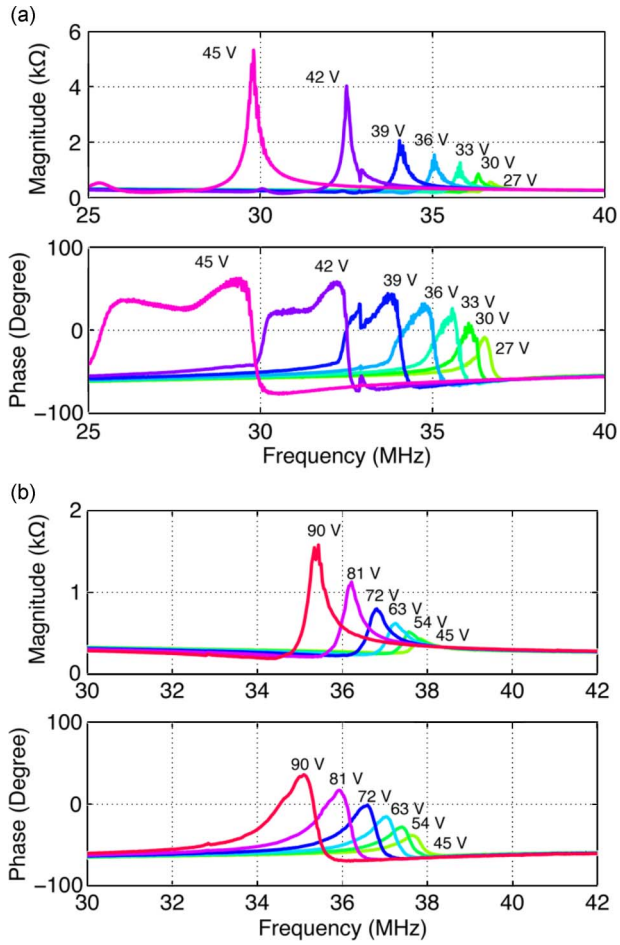

Fig. 9. Electrical input impedance of two devices in air. These devices have a plate radius of 6 μm and a thickness of 0.5 μm with (a) 40-nm gap and (b) 130-nm gap. A resonant frequency reduction due to the spring softening effect is clearly visible.

coupling between the elements [Fig. 8(a)]. Each element was made of hundreds to thousands of cells depending on the design, all electrically connected in parallel [Fig. 8(b)]. The bonding area between the cavities is 4 μm, and at the edge, it is 12 μm to ensure good vacuum sealing. The defined shape of the silicon plate [curved, Fig. 8(b)] is a result of the goal of minimizing the parasitic capacitance at the oxide post area.

B. Characterization

We measured the electrical input impedance (Model 4294A, Agilent Technologies, Palo Alto, CA) to verify for functionality and device characteristics, such as the resonant frequency and quality factor. From both wafers, i.e., with 40-nm and 130-nm gap heights, we only measured devices with 1000 cells with 6 μm radius each (Fig. 9). For these electrical input impedance measurements, different dc bias voltages were applied up to the pull-in point, according to the gap height. As expected, with increasing dc bias voltages, the resonant frequency drops due to spring softening effect [Figs. 9 and 10(a)], while the magnitude of the electrical impedance (proportional to the mechanical response) increases.

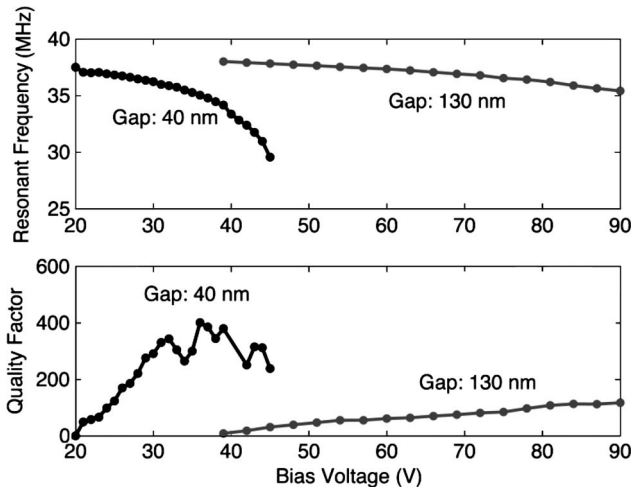

Fig. 10. Comparison of two devices with different gap heights. The resonant frequency and the quality factor are calculated from the measurements shown in Fig. 9.

Based on these impedance measurements, which consist of contributions of 1000 plate resonators, all connected in parallel, we calculated the parallel resonant frequency [Fig. 10(a)] and

quality factor at the resonant frequency [Fig. 10(b)]. For the device with a 40-nm gap height, we measured an impressive quality factor of 400. These input impedance measurements demonstrate that the devices with 40-nm and 130-nm gap heights were successfully fabricated and fully functional ($> 90\%$ yield).

IV. Discussion

Our results demonstrate that direct bonding on a selectively grown thermal oxide (LOCOS) without a chemical-mechanical polishing step can be used to fabricate MEMS-based ultrasonic devices. The measured high quality factor indicates the quality of the bond interface because it allows maintaining vacuum-sealed cavities, even with only 15 μm wide bonding area. The fabricated devices feature low dc bias voltage requirement due to the small gap height and the extend post generated by the LOCOS process. Advantages are the increased design flexibility, because one can design the height of the gap and the thickness of the post independent to each other. In general, our measurements prove that the devices with a high ratio ($\sim 1:18$) between the gap height and the oxide post thickness can be realized.

The key feature of this process is the feasibility of direct wafer bonding on a locally grown oxide. We control each step of the process to fulfill the bonding criteria, the surface roughness, and the wafer flatness. In terms of the surface roughness, the location of the bonding area needs extra protection. We achieve this by not exposing the later bonding area to any plasma etching. Instead, we only use wet etching with minimum over-etching time. First, when we pattern the grown oxide [Fig. 2(a)], we etch only 90% of the oxide with plasma etching. Then, the remaining oxide is removed with 6:1 BOE with 30-s overetching time. Second, we choose the thicknesses of the two consecutive oxidations as described in the previous section to minimize the exposure time of the postregion to 6:1 BOE [Fig. 2(c)]. Third, we use a thin oxide layer as etch stop, when we pattern the nitride layer by plasma etching [Fig. 2(e)]. Due to all of these precautions, we observe an increase of the surface roughness from 1.8 (bare silicon wafer) to 2.36 Å_{RMS} (oxide post before wafer bonding). In addition to surface roughness, locating the same amount of stress-inducing layer, such as a thermally grown oxide, on both sides of the wafer, affects the wafer curvature. First, we remove the oxide on both sides of the wafer after performing two consecutive oxidations [Fig. 2(c)]. Thus, the wafer at this step is in a stress-free condition. Second, during the LOCOS step [Fig. 2(f)], the same amount of oxide is grown on both sides of the wafer, which again results in a stress-balanced wafer condition before the wafer-bonding step. As a result, we achieve a wafer with a minimal curvature of 10 μm across the entire wafer. In case the portion of the cavity area cannot be neglected in terms of the wafer curvature, the oxide on the backside can be partially removed to balance the stress.

The described process supports a wide range of geometries. However, there are some limitations in terms of lateral and vertical dimensions. The thermal oxidation process limits the vertical dimension, i.e., the thickness of the oxide post and the height of the silicon bump. Because typical thermal oxidation processes at atmospheric pressure limit the oxide thickness to few micrometers, the dimensions are limited to a similar range. Such limitations can be addressed by using a high-temperature high-pressure oxidation techniques. However, the effect of the oxidation process on the surface roughness must be considered as well. In addition, the lateral dimensions, i.e., the radius of the silicon bump and cavity, are related to the thickness of the consecutive oxidation steps. As shown in Fig. 2(c), the oxidation results in a round-shaped edge of the bump and, thus, reduces the flat active electrode area. As a result, the thickness of the oxide limits the minimum radius of the silicon bump. As aforementioned, the radius of the cavity, i.e., the radius of the resonator, has to be larger than the radius of the silicon bump by a certain amount. Therefore, the two consecutive oxidation steps limit the minimal radius of the plate as well.

As shown in the previous section, we fabricated two devices with different gap heights. First, the more aggressive design has a gap height of only 40 nm. To the authors' knowledge, this is the smallest gap height demonstrated in a CMUT so far. For a second design, a 130-nm gap was fabricated as a backup device. The successful measurement results obtained from both devices demonstrate the benefit of the 40-nm-gap device. At low dc bias voltages, the parasitic capacitance loads the device, and thus, it degrades the quality factor in the input impedance measurement. As a result, the quality factor increases with dc bias voltages until the device has a high electromechanical coupling. If the device has a high electromechanical coupling, the loading due to the parasitic capacitance becomes negligible, and the measured quality factor represents the mechanical quality factor of the device. In the measurement [Fig. 10], the 40-nm-gap device has a high quality factor (300–400) starting from 32 V. However, the 130-nm-gap device is still affected by the parasitic capacitance loading at dc bias voltages up to 100 V.

The target application for the fabricated devices is resonant chemical sensing based on mass loading effect [11]. The motivations of using a CMUT as a chemical sensor are the following: 1) exploiting the parallelism of the structure, which exhibits a large active detection area; and 2) a high quality factor due to the vacuum cavity beneath the moving plate. In order to archive a high quality factor for a flexural mode resonator in air, the so far demonstrated approach is based on reducing the size of the resonator down to the comparable size of the mean free path in air at 1 atm [24]. Even though this achieves the same quality factor, the active area is significantly reduced as well. As a consequence, the sensor will interact with lower number of gas molecules. This is not the case in our device, due to the inherent parallelism resulting in a huge active detection area. Thus, our 40-nm-gap device shows a high quality factor of 400 at a high resonant frequency of 43 MHz (Fig. 10). This is possible due to the peripheral support of our resonant plate and the vacuum cavity beneath. Further, the device offers a lightweight resonant structure, which is only 500 nm thick, and a large detection area of 1.13×10^5 μm^2. Accordingly, this device is a promising candidate for resonator-based mass sensor applications, such as chemical/biological sensor applications. For future work, we plan to use these devices for such experiments.

Further, we repeatedly measured such high quality factors for these devices over a time period of over the last three years. This demonstrates that high-temperature-assisted direct wafer bonding on a locally grown oxide can be done without any drawbacks.

V. Conclusion

This paper has presented a fabrication process of a direct wafer-bonded CMUT based on LOCOS. Our results have proved that this fabrication process offers precise gap height control, which is independent of the oxide post thickness. Therefore, we have demonstrated a CMUT with an unprecedented small gap height of only 40 nm but with a thick oxide post of 720 nm. Such a high ratio between the post and gap height not only features high reliability but also eliminates the need for high dc bias voltages. In addition, we have demonstrated the successful high-temperature-assisted direction wafer bonding to the locally grown oxide without any chemical-mechanical polishing. The CMUT fabricated by this process can be utilized for chemical and biological sensor platform with advantages such as thin resonant structures (500 nm), high quality factor ($\sim$400), and high resonant frequency ($\sim$43 MHz) in air. In addition, this process flow will help to realize efficient wafer-bonded CMUTs for various ultrasound applications (e.g., medical imaging) featuring high reliable operation due to the extended insulation layer structure.

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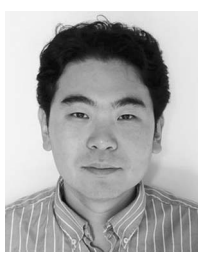

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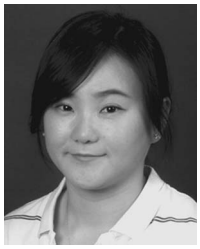

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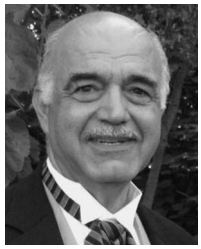

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