

Large Area 1D CMUT Phased Arrays for Multi-Modality Ultrasound Imaging

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Abstract – We present the design and fabrication of 1D capacitive micromachined ultrasonic transducer (CMUT) arrays optimized for imaging using multiple modalities. A new variation of the fabrication process based on a thick buried oxide layer is used to build these CMUTs. In our process, the via connections for each cell's electrode with the handle layer are made from the front side. This enables fabricating CMUT cells with smaller sizes, and higher resonant frequencies. Initial characterization results agree well with our design simulations.

Keywords: CMUT, thick-BOX process, multi-modality imaging, MEMS

I. INTRODUCTION

Capacitive Micromachined Ultrasound Transducers (CMUTs) offer many advantages over conventional piezoelectric transducers. CMUTs inherently have a large bandwidth (in immersion). Unlike piezoelectric transducers, they do not overheat when delivering ultrasound energy over a prolonged period of time. These qualities make CMUTs ideal for use in multi-modality medical ultrasound imaging with techniques like harmonic imaging, ultrafastTM imaging and shearwaveTM elastography.

In this work, we have designed and fabricated 1D CMUT phased arrays for cardiac and trans-thoracic multi-modality ultrasound imaging. The CMUTs were designed using an equivalent circuit model [1, 2] and fabricated using a modified version of the fabrication process [3] developed by Kupnik et al. to improve the device performance and reliability. In our process, the via connections for each cell's electrode with the handle layer are made from the front side. Also, we use a low temperature wafer bonding process with an intermediary titanium layer [4-6] for bonding the plate wafer instead of high-temperature assisted direct wafer bonding.

II. DESIGN

Different ultrasound imaging modalities dictate different requirements on the ultrasound transducer. For example, harmonic imaging requires a transducer with a high bandwidth and shearwaveTM elastography [7] requires a transducer with a high transmit pressure for creating the shear waves. When generating high acoustic pressures, it is also necessary to have

a high efficiency and good thermal behavior. This makes it challenging to design a single transducer that can simultaneously satisfy these requirements and be used for ultrasound imaging using multiple modalities. We designed a large area ultrasound transducer array optimized for cardiac and trans-thoracic imaging using conventional B-mode imaging along with tissue harmonic imaging, shearwaveTM elastography and ultrafastTM imaging.

As a first attempt at making multi-modality ultrasound transducers, we designed 1D CMUT phased arrays. Cardiac imaging requires a transducer with large imaging depth of at least 15 cm. Hence a lower resonant frequency was selected. Two types of arrays were designed with 64 and 80 elements each and an element pitch of 280 μm and 224 μm respectively. Both arrays were designed to have the same basic cell (Fig 1), for ease of fabrication on a single wafer. The arrays were designed to have an element height of 14 mm. The CMUTs were modeled with an equivalent circuit model [1, 2] and simulated for computation of bandwidth and output pressure. In immersion in water, these arrays would have a -3 dB bandwidth of 1 MHz to 6 MHz (Fig. 2(a)).

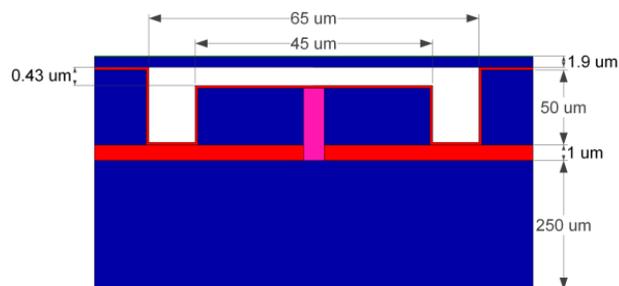


Fig. 1. Basic CMUT cell design

The CMUT cells have been designed to pull in (collapse) at 200 V. When biased at 80% of this voltage and excited by an a.c. signal of 80 V amplitude, this CMUT can generate 630 kPa of acoustic pressure in water.

A low noise preamplifier from MAXIM (MAX 4805A) was considered along with a standard coaxial cable in the simulation to determine the noise performance of the entire system. We expect both arrays to have a minimum noise figure of less than 9 dB (Fig. 2(b)). The amplifier which will

be integrated in the probe handle will overcome the limitation of electrical impedance mismatch between the CMUT element and the coaxial cable.

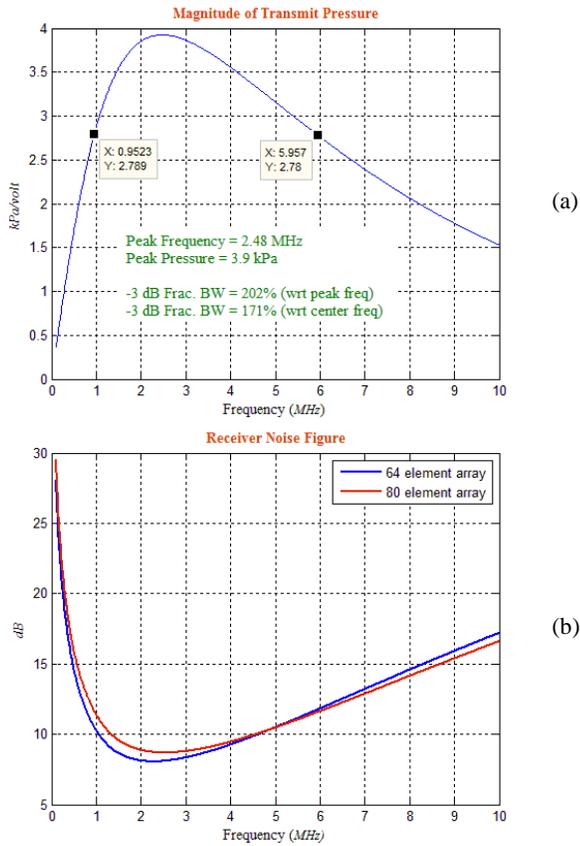


Fig. 2. Linear model simulation results (a) TX pressure and bandwidth when immersed in water (b) RX noise figure with MAX4805A high-voltage-protected, low noise op-amp for in-probe use in ultrasound applications

III. FABRICATION PROCESS

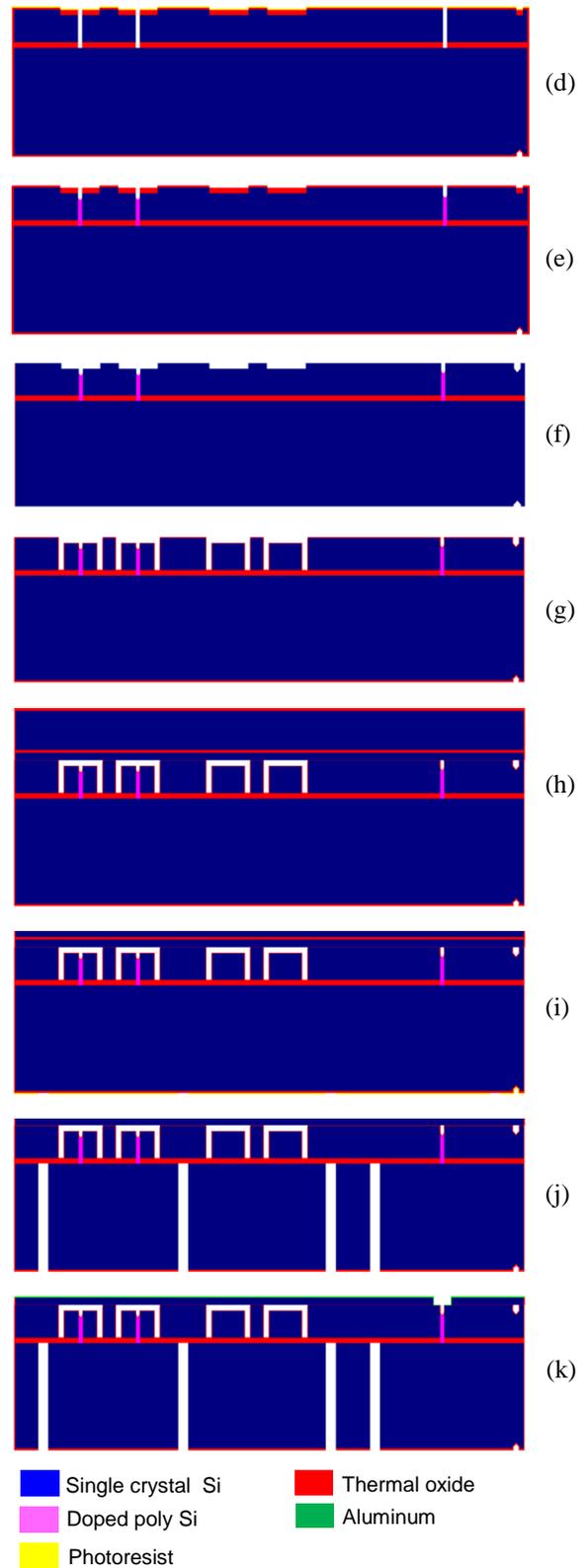
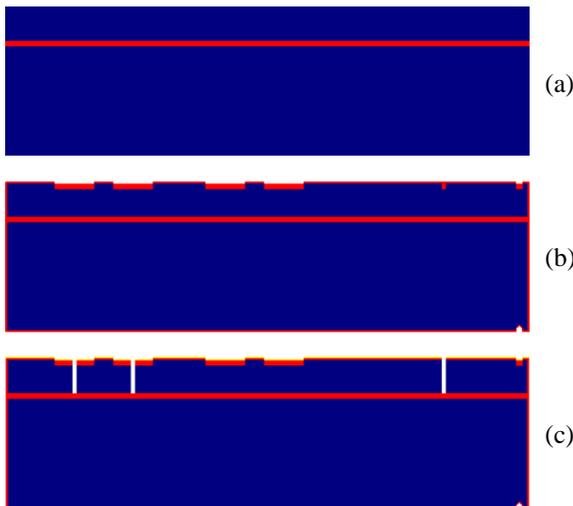


Fig. 3. Fabrication process flow

The devices were fabricated on an SOI wafer (Fig. 3(a)) with a 1 μm thick buried oxide (BOX) layer. The device layer and handle layer thicknesses were chosen to be 50 μm and 250 μm

respectively. These thicknesses allow etching the deep high aspect ratio holes and trenches required for this design. At the same time, the 300 μm total thickness of the wafer provides sufficient mechanical strength allowing convenient handling of the wafer during fabrication.

The SOI wafer was first oxidized and patterned to define the CMUT cells. Then a subsequent oxidation step was carried out. The oxide barrier causes a differential oxidation rate between the patterned and non-patterned region. The difference in oxidation depth determines the gap height in the CMUT cells (Fig. 3(b)).

Next, 4 μm wide vias were etched from the front side using DRIE (STS HRM deep RIE etcher) (Fig. 3(c)). The BOX layer at the bottom of the vias was etched in a 2% HF solution to open up contacts to the underlying substrate (Fig. 3(d), Fig. 4). The vias were then filled with poly silicon (LPCVD at 620 $^{\circ}\text{C}$), and doped by diffusion with an n-type dopant (POCl_3 at 1000 $^{\circ}\text{C}$) to establish an electrical connection. The poly silicon on the wafer surface was then etched back with a plasma etcher (Drytek model-100) (Fig. 3(e)), and the oxide was stripped off using a 6:1 BOE solution (Fig. 3(f)).

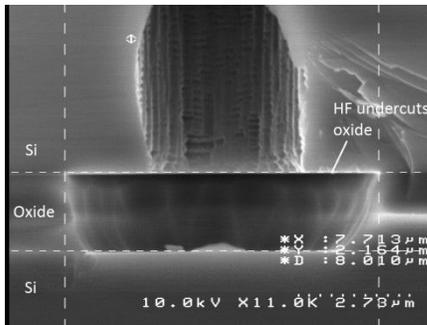


Fig. 4. SEM image of a via hole with buried oxide layer etched with 2% HF solution

Donut shaped trenches were etched on the front side using DRIE (STS HRM deep RIE etcher) which define the bottom electrode for each cell of the CMUT. A 450 nm thick insulation oxide layer was thermally grown in a furnace at 1100 $^{\circ}\text{C}$ (Fig. 3(g)).

To create the plate of the CMUT cell, an SOI wafer which has a 1.9 μm thick device layer was then bonded with the original SOI wafer with an intermediary titanium adhesion layer [4-6] (Fig. 3(h), Fig. 5) using a process developed by Tsuji et al [4]. The plate wafer was then thinned down using isotropic plasma etching. (Fig. 3(i))

Individual elements in each array were then isolated using DRIE on the back side (Fig. 3(j)). The remaining handle layer and BOX layer of the plate wafer were then etched away using RIE to release the plate. Further, the plate was patterned and etched to open contacts to each element from the front side. A

100 nm thick layer of aluminum was then evaporated on top of the plate to increase the conductivity (Fig. 3(k)).

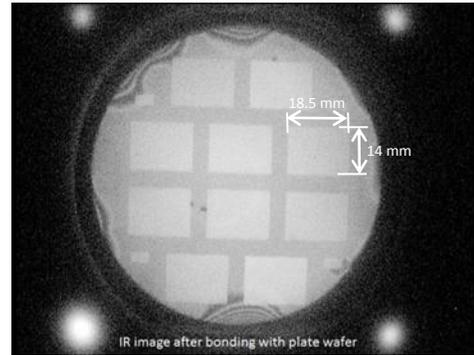


Fig. 5. Infrared image after bonding with the plate wafer, showing void-free bond across the wafer, except some unbonded area near the edge

IV. PRELIMINARY RESULTS AND DISCUSSION

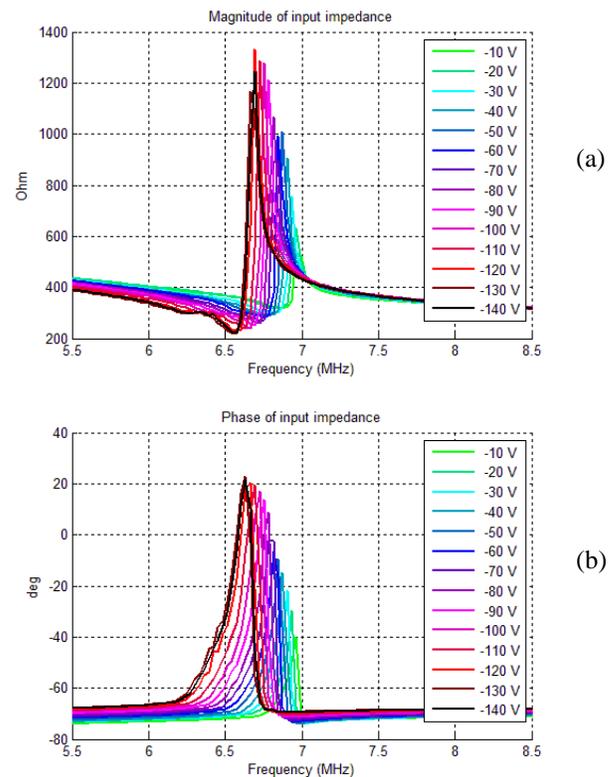


Fig. 6. Electrical input impedance measurements [(a) Magnitude (b) Phase] of a CMUT element biased up to 70% of pull-in voltage

The fabricated CMUT arrays were tested in air. The collapse voltage for these devices was measured at 200 V, as per design. The input impedance measurements (Fig. 6) confirmed a resonant frequency of ~ 7 MHz in air. The total device capacitance was computed from the input impedance measurements to be 76 pF. Out of this, 44 pF comes from the capacitance across the buried oxide while the remaining 32 pF

comes from the CMUT cells. This is in close agreement with the simulations, which predicted the total active and parasitic capacitance from the cells to be ~ 30 pF.

After fabrication, the devices are fragile due to the $250\ \mu\text{m}$ deep element isolation trenches on the back side. This makes it challenging to singulate individual arrays from the wafer. Also this poses additional challenges for assembling the arrays into ultrasound probes. We are currently working on improving the mechanical strength of these devices. This can be achieved by filling the trenches with some dielectric material, or by bonding to a stiffer substrate wafer.

V. CONCLUSIONS

We designed a 1D CMUT array capable of imaging using multiple modalities simultaneously. These arrays were manufactured using a modified version of the fabrication process based on a thick buried oxide layer. Preliminary characterization results match closely with our simulations.

Being able to make via connections from the front side prior to wafer bonding opens up possibilities for smaller geometry and higher operating frequencies for the thick BOX process for fabricating CMUTs. However new approaches need to be explored for mechanical strengthening of such CMUT arrays.

ACKNOWLEDGMENTS

This work was supported by SuperSonic Imagine, France under the scope of the ICARE project. The devices were fabricated at the Stanford Nanofabrication Facility (a member of the National Nanotechnology Infrastructure Network). We thank Dr. Nicolas Felix and Francois Maurice, Supersonic Imagine, France for our many fruitful discussions. We also thank Vermon SA for carrying out measurement tests.

REFERENCES

- [1] I. Wygant, M. Kupnik and B. T. Khuri-Yakub, "Analytically calculating membrane displacement and the equivalent circuit model of a circular CMUT cell" in Proc. IEEE Ultrasonics Symposium, pp. 2111-2114, 2008
- [2] A. Lohfink and P. C. Eccardt, "Linear and nonlinear equivalent circuit modeling of CMUTs" in IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, vol. 52, no. 12, pp. 2163-2172, 2005
- [3] M. Kupnik, S. Vaithilingam, K. Torashima, I. Wygant, and B. T. Khuri-Yakub, "CMUT fabrication based on a thick buried oxide layer" in Proc. IEEE Ultrasonics Symposium, pp. 547-550, 2010
- [4] Y. Tsuji, M. Kupnik, and B. T. Khuri-Yakub, "Low temperature process for CMUT fabrication with wafer bonding technique" in Proc. IEEE Ultrasonics Symposium, pp. 551-554, 2010
- [5] Yu Jian, Wang Yinmin, Lu Jian-Qiang, Gutmann Ronald J, "Low-temperature silicon wafer bonding based on Ti/Si solid-state amorphization" in Appl. Phys. Lett., 89,092104, 2006
- [6] Jian Yu, Yinmin Wang, Arthur W. Haberl, Hassa Bakhru, Jian-Qiang Lu, Ronald J. Gutmann "Mechanisms of Low-Temperature Ti/Si-Based Wafer Bonding," In Materials, Technology and Reliability of Advanced Interconnects Symposium (Materials Research Society Proceedings Vol.863), pp. 387-92, 2005
- [7] Jeremy Bercoff,, "ShearWaveTM Elastography" white paper from www.supersonicimagine.fr