Wafer-bonded CMUT meets CMOS
MEMS-based Ultrasonic Transducer Arrays including Electronics Integration

Mario Kupnik and Butrus T. Khuri-Yakub

Edward L. Ginzton Lab, Stanford University, CA

www-kyg.stanford.edu
Outline

- **Capacitive Micromachined Ultrasonic Transducers**
  - Background, how it works, how it’s made, and for what it can be used.
  - What was done for CMOS integration so far.

- **Latest 2D array fabrication process (THICK-BOX)**
  - Research towards high-reliability CMUTS with high performance.

- **Integration to CMOS via low-temperature bonding.**

- **“Substrate-less” CMUT fabrication – CMOS will help.**

- **Conclusions and Outlook**
“After a month of careful study, during which both magnetostriction and piezoelectricity were considered and then rejected, Langevin decided that it would be safer to fall back on the “singing condenser”... (March 1915). Numerical estimates indicated that, if electric field strengths of the order of a million volts per centimeter ($10^8$ Volt per meter or 100 V per micron) could be maintained, electrostatic forces as large as a kilogram per square centimeter would (theoretically) come into play...”


For $E = 300$ V per micron, the electrostatic force is equal to what $B = 1$ Tesla can create!

(Large hadron collider at CERN, Geneva, uses up to $B = 8.3$ Tesla)
Capacitive Transducer – The basic idea is simple

\[ W(Q, d) = \frac{1}{2} \frac{Q^2 d}{\varepsilon_0 A} \]

\[ F_{el} = \frac{1}{2} \varepsilon_0 A \frac{V^2}{d^2} \]

Quadratic distortion at twice the frequency

\[ F_{el} = \frac{C^2 V_{AC}^2}{4 \varepsilon_0 A} \left(1 - \cos 2\omega t\right) \]
Capacitive Transducer – Why we need a DC bias voltage

\[ W(Q, d) = \frac{1}{2} \frac{Q^2 d}{\varepsilon_0 A} \]

\[ F_{el} = \frac{1}{2} \varepsilon_0 A \frac{V^2}{d^2} \]

\[ F_{el} = \frac{C^2}{2 \varepsilon_0 A} \left( V_{DC}^2 + 2 V_{DC} V_{AC} \sin \omega t + \frac{V_{AC}^2}{2} \right) \]

Linear and magnified by \( V_{DC} \)

Static force component

Quadratic distortion
The first CMUT was an air transducer (Haller, Khuri-Yakub, 1994)

The complete transducer is micromachined, i.e. also the moving part (“membrane”).

Frequency range: 1.8 MHz ... 4.6 MHz
3 dB fractional bandwidth: 20 %
CMUTs can be used for both airborne ultrasound and immersion.

**Equivalent Circuit Model:**

- **Electrical Domain:**
  - $I_{AC}$
  - $V_{AC}$
  - $R_{series}$
  - $C_p$
  - $C_o$

- **Mechanical Domain:**
  - $Z_{plate}$

- **Graphs:**
  - **Magnitude of Pressure in Air**
    - $f_1 = 9.91$ MHz
    - $f_2 = 9.99$ MHz
    - $f_c = 9.95$ MHz
    - FBW = 0.875%
  - **Magnitude of Pressure in Water**
    - $f_1 = 1.9$ MHz
    - $f_2 = 17.1$ MHz
    - $f_c = 9.5$ MHz
    - FBW = 158%
Microelectronics industry gave us all tools that we needed

Using this technology, various devices were fabricated...

- Circular cells
- Hexagons
- Tents

Devices fabrication and photos by Prof. Arif Sanli Ergun.
Monolithically integrated CMUTS so far

However, CMUTs fabricated with sacrificial release process suffer from several drawbacks, in particular when low temperature processes are used.

E.g.: Non-uniformities, low reproducibility, intrinsic stress, gap height limits due to roughness, etc.

Chip-bonding after CMUT is finished is a good approach, but there are still weak points present related to sacrificial release process.
Let’s get the best out of the CMUT first before we think CMOS

1. Grow thermal oxidize on silicon wafer
2. Pattern oxide, this step defines cell diameter
3. Grow thin oxide at bottom of cavity
4. Perform fusion Bonding step to SOI wafer
5. Remove handle wafer and BOX layer

Wafer-bonded CMUTs and electronics integration so far

Trench-frame 2D CMUT array solder bumped to IC

This way, many arrays can form a large imaging device

Trench-frame CMUTs solder bumped to interposer solder bumped to IC

Elvis Lin, et al, 2009

However, this is problematic for thin-gap devices

10 nm average displacement at 10 MHz in immersion translates into 1 MPa acoustic pressure

\[ F \sim E C_0 V_{AC} \]

Electrical breakdown and high parasitic capacitance

This fabrication process solves the issue and features many advantages

One of the main advantages is a high electrical breakdown voltage.

**Optimized cell:** The insulation layer thickness at the gap and at the post are completely independent from each other - ultra high reliable device in terms of electrical breakdown with low parasitic capacitance.

**Example:** Effective oxide at the gap can be 100 nm and at the post area several microns.

Due to the thick BOX layer at the post area, the chance of electrical breakdown is significantly reduced, as well as the parasitic capacitance - more reliable device with better performance.

Front view of cross-section of one cell
Several options how to merge CMUT wafer and CMOS wafer

- Under bump metallization for chip bonding (die or wafer level)

- Metal layers for eutectic bonding (Au-Si, 365°C) [13], [14]

- Metal layers for thermo compression bonding (Ti-Au, 300°C) [15]

- Low temperature fusion bonding, e.g. [16] (Mitsubishi and AML sell such tools, Ziptronix)
Low temperature fusion bonding is state-of-the-art:

For example: This fully-automated room-temperature bonding tool (8”) from Mitsubishi Heavy Industries Ltd., Japan, features covalent bond strength at room temperature.

It uses ion beam surface activation technique under high vacuum condition.
We also pursue a second approach – substrateless CMUT, for example:

1. Deposit LTO on CMOS substrate + CMP
2. Low-temperature fusion bond to SOI to transfer single crystal silicon plate
3. One lithography and etch cavities
4. Single cell access
5. Several cells connected in parallel

Conclusions

- Wafer-bonded CMUTs and CMOS are compatible!
  - Required to get the best from both worlds – Wafer-bonded CMUTs monolithically integrated.

- For large and medium size 2D arrays, this approach will allow to develop the next generation medical imaging probes and therapeutic transducers (HIFU) at low cost without expensive and complex interposer solutions.

- At the moment we pursue research for direct monolithic CMUT integration on top of a CMOS-circuitry-containing substrate, i.e. CMOS wafer acts as substrate for a wafer-bonded CMUT fabrication process.
References

Acknowledgements

Srikant Vaithilingam, Stanford University
Kazutoshi Torashima, Canon Inc.
Ira O. Wygant, National Semiconductor
Yukihide Tsuji, NEC Inc.
Michael Cernusca, AVL List GmbH
Kudlaty Katarzyna, AVL List GmbH
Steve Vargo, SPP Process Technology Systems, Inc.

This research was funded by following research partners:

(in alphabetical order)

AVL List GmbH, Graz, Austria
Canon Inc., Tokyo, Japan
Thank you and for more information feel free to contact us

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Mario Kupnik
Senior Research Scientist
E. L. Ginzton Laboratory, room 49
Stanford University
Stanford, CA 94305-4088
Office: +1-650-725-4942
kupnik@stanford.edu

Butrus (Pierre) T. Khuri-Yakub
Professor
E. L. Ginzton Laboratory, room 11
Stanford University
Stanford, CA 94305-4088
Office: +1-650-723-0718
khuri-yakub@stanford.edu