

Low Temperature Process for CMUT Fabrication with Wafer Bonding Technique

Yukihide Tsuji, Mario Kupnik, and Butrus T. Khuri-Yakub

Abstract—We present the successful fabrication of capacitive micromachined ultrasonic transducers (CMUTs) based on low temperature wafer bonding (< 400°C). Such a fabrication process enables the direct integration of CMUTs on top of IC substrates, and requires only two additional lithography steps for fabricating the complete CMUT. Our approach benefits from both the integrated electronics and the well-controlled performance of CMUTs with single-crystal silicon plates. The yield of the CMUTs is almost 100%, and the standard deviation of resonance frequency in air is less than 1% in the whole 4 inch wafer.

Index Terms—Capacitive micromachined ultrasonic transducer, monolithic integration, low temperature process, wafer bonding.

I. INTRODUCTION

THREE-dimensional (3D) ultrasound imaging provides clinical benefits to less difficult and less expensive examinations beyond those of traditional two-dimensional (2D) ultrasound imaging [1]. On the other hand, 2D arrays for 3D imaging have a very large number of elements, which enhances the difficulty of packaging as well as data processing. The integration of ICs and transducers gives a solution to these problems [2-8].

Capacitive micromachined ultrasound transducer (CMUT), one of the transducers, can be fabricated with photolithography and other mature techniques built up in semiconductor industries [9]. When CMUT arrays are fabricated on a silicon substrate, the electrical contact to each element of CMUTs is needed from the back side through the thick substrate (~300 um); through-wafer via [10-12] and through-wafer trench isolation [13] technique. These connecting processes are so complicated that the process cost increases.

Direct fabrication of CMUT on the substrate with ICs eliminates the complicated connection process, but the process temperature is limited under 400°C to avoid severing the metal connections in the ICs. Some researchers demonstrated the fabrication with sacrificial release process including selective

etching and shield processes [14-17]. The limited temperatures degenerate uniformity and reproducibility of deposited films.

Crystal transfer technique with wafer bonding is useful for preparing a single-crystal silicon plate as a membrane of CMUT [18]. The process temperatures of wafer bonding and post-annealing were usually very high (~1000°C). One approach to decrease the temperature is to activate the surface by creating many dangling bonds. For example, the temperature to bond Si to SiO has been decreasing down to room temperature with in-situ plasma ion exposure [19]. Another approach is to deposit the material which migrates into silicon at lower temperatures, e.g. titanium [20-21] and gold [22]. Titanium has been used in back end of line (BEOL), and it migrates to silicon at 400°C under moderate pressure. The migration also reduces the acceptable level of surface roughness on the substrate compared with that in the former approach. Therefore titanium to silicon wafer bonding technique has a great potential in monolithic integration of CMUTs [20].

We fabricated CMUTs with the wafer bonding process at 400°C using titanium thin film as an adhesion layer. The process requires only two additional lithography steps for fabricating the CMUT on top of IC substrates. The electric impedance in air was measured, and it was characterized with a 1D equivalent circuit model.

II. RESULTS

A. Process Flow

Figure 1 shows the process flow to fabricate CMUT on a silicon substrate. All processes are done under 400°C. Thus, the developed process is available for the substrate with ICs. First, silicon oxide (86 nm) is deposited on a silicon substrate by low pressure chemical vapor deposition at 400°C (Tylan; Tystar Corporation, Torrance, CA). Then the low temperature oxide (LTO) is etched for via contact to the silicon substrate (P5000; Applied Materials, Santa Clara, CA), and titanium is deposited by DC-magnetron sputter (Gryphon, Gryphon products, Hayward, CA) [Fig. 1 (a)-(b)].

Titanium film is used for the via-contact as well as for an adhesion layer on wafer bonding. Both titanium and LOT layers are etched by P5000 [Fig. 1 (c)]. The formed gap is for a cavity of CMUT. The patterned substrate and a blank SOI wafer are bonded together at 400°C with 2.5 kN down-force in vacuum (<10⁻⁴ Torr) for 2hour (EVG510; EVG, Tempe, AZ) [Fig. 1 (d)]. The silicon of SOI wafer had been heavily doped

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by diffusion with phosphorus dopant to achieve doping levels required for ohmic contact from both front- and back-side of SOI. The doping was performed at atmospheric pressure at 1050°C for 30 minutes in a furnace (Tylan). After diffusion, the wafer was annealed at 1050°C in a nitrogen environment for one hour. The substrate was cleaned with 50% HCl (H₂O:HCl=1:1) in 45 sec, and SOI was done with DHF (H₂O:HF=50:1) in 30 sec just before bonding. The surface roughness of the substrate was checked by atomic force microscope (Fig. 3). The root mean square (RMS) roughness increases up to 1.66 nm after depositing LTO and titanium. The bonding strength, however, is enough to follow processes including grind and dicing process. The acceptable RMS value on wafer bonding is much high compared with that in SiO-Si bonding (0.5 nm) [23]. This is caused by that Ti and Si easily migrate through the bonding interface under the moderate pressures and temperatures.

The backside silicon of the bonded SOI wafer is thinned down to 100 μm, and the left silicon and bottom oxide of the SOI wafer are removed by wet etching; a heated tetramethylammonium hydroxide (TMMA) for silicon, and a buffered oxide etchant (BOE) for BOX. Therefore, a thin crystal silicon plate (330 nm) remains on the LTO as well as on the air gap with the support of the surrounding bonded area [Fig. 1 (e)]. The silicon plate is separated into elements (250 μm x 250 μm) by dry etching (Drytek, General Signal Corp., Stamford, CO). In this time, titanium layer is used as an etch-stopped layer. The remained titanium on LTO is removed by Piranha etchant (H₂SO₄: H₂O₂= 9:1, 90°C) utilizing the silicon plate as a mask [Fig. 1 (f)]. Following LTO etching is for another contact to the substrate (Drytek) [Fig. 1 (g)]. Finally titanium (20nm) and aluminum (400nm) are deposited and

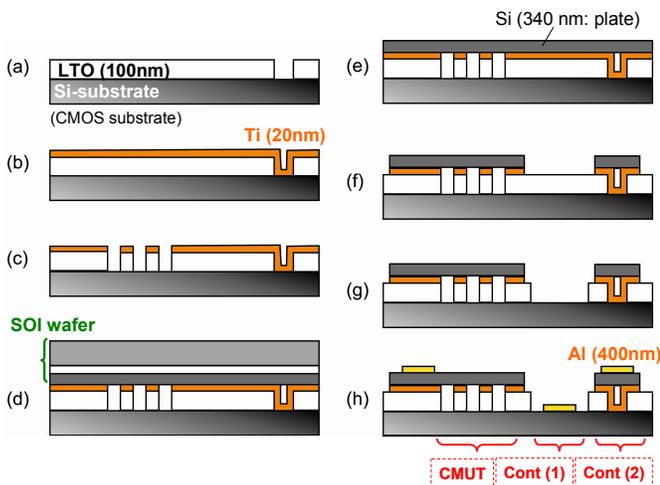


Figure 1: Process flow. (a) LTO deposition and etching for via contact, (b) Titanium deposition, (c) LTO and titanium etching for gap of CMUT, (d) Wafer bonding, (e) Backside silicon and bottom oxide of SOI etching, (f) Silicon plate and titanium etching to separate each elements, (g) LTO etching for ground contact, (h) Aluminum deposition and etching for metal pads .

pattered by wet-etchant for metal pads [Fig. 1(h)].

In the process flow, we showed the two ways of electrical contact to bottom electrode (=silicon substrate). The resistance of Ti-via (10 μm x 10 μm) can be measured (about 25 Ohm) with the two type contact. Titanium is found to also have a good electrical contact to the bonded Si plate (top electrode).

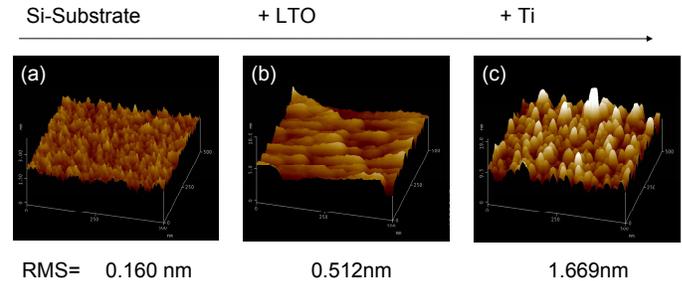


Figure 2: Root mean square (RMS) roughness on (a) the surface of a silicon substrate, (b) that after LTO deposition, and (c) that after titanium deposition following LTO deposition.

B. Device structure and measurement methods

Figure 2 shows the structure and its parameters of CMUT. Silicon plate thickness is 330 nm, which is equal to SOI thickness. Radius of cavity is 6, 8, and 10 μm, and the resonance frequency in air is decreased with increase in the radius (34, 22, and 16 MHz). Depth of cavity (111 nm) is almost equal to summation of Ti (20 nm) and LTO (86 nm) thicknesses. 5 nm of silicon substrate was over-etched during LTO etching.

The electrical impedance of the CMUT in air is measured with Agilent 4294A. The results are compared with simulation results obtained by a 1D equivalent circuit model, where the circuit parameters are calculated using displacement profile of plate and the piston model of the plate [24].

Element size (Lx, Ly)	Plate thickness (T)	Gap (d)	Cavity		
			Pattern	Size (R)	Pitch
250 x 250 μm	330 nm	111 nm(*)	Circle	10μm, 8μm, 6μm	1.5 x (cavity size)

(*) 111nm= 86 nm (SiO) + 20 nm (Ti) + 5nm (over-etching) .

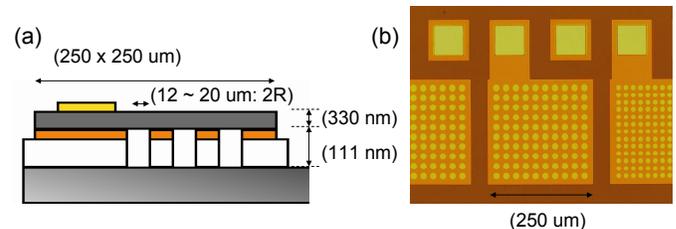


Figure 3: Device structure and its parameters. (a) Side view and (b) Top view (picture).

C. Impedance measurement in Air

An electrical impedance of CMUT in air is measured. A resonance peak appears when applying DC bias between top and bottom electrodes as shown in Fig. 4 (a)-(b). The measured impedance can be fitted with the circuit parameters shown in Fig. 4 (c). Through an electromechanical constant, current is correspond to the velocity of silicon plate, L_m is to the mass, $1/C_m$ is to the spring constant, and R is to the damping factor. C_p is parasitic capacitance and R_p is series resistance.

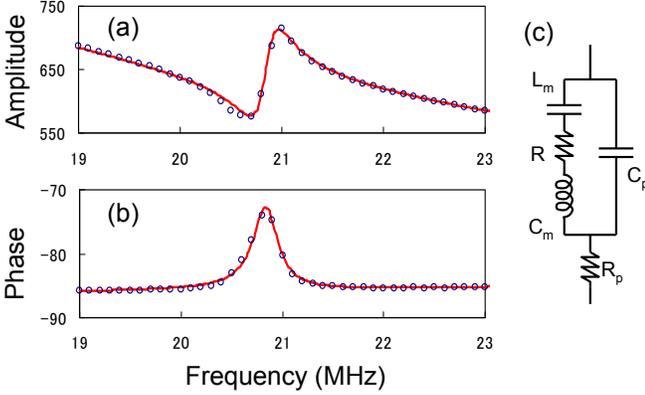


Figure 4: Electrical impedance of CMUT; (a) Amplitude, (b) Phase. The radius of cavity is 8 μm . DC bias is 12 V. Plots are experimental results. (c) Circuit parameters for fitting. Solid line in Fig. 4 (a)-(b) is fitted lines with the circuit parameters. $L_m = 1.56 \times 10^{-3}$ [H], $R = 2650$ [Ohm], $C_m = 2.35 \times 10^{-14}$ [C], $C_p = 1.20 \times 10^{-14}$ [F], $R_p = 50.9$ [Ohm],

Figure 5 (a) shows the dependence of electrical impedances on DC bias voltage. The resonance frequency decreases with increase in DC bias as shown in Fig. 5(b). It is caused by the electromechanical interaction, and called spring softening effect [25]. In Fig. 5(b) the simulation results with a 1D equivalent circuit model are also showed by solid lines. The simulation reproduces the results of resonance frequency well. Fig. 5 (c)-(d) shows L_m and C_m obtained by fitting. The lines are the simulation results. Both L_m and $1/C_m$ of simulation results are 35 % smaller than those of the measured results. It indicates that mechanical electrical constant and/or effective movable area might be 35 % underestimated in the simulation when using a piston model of the plate.

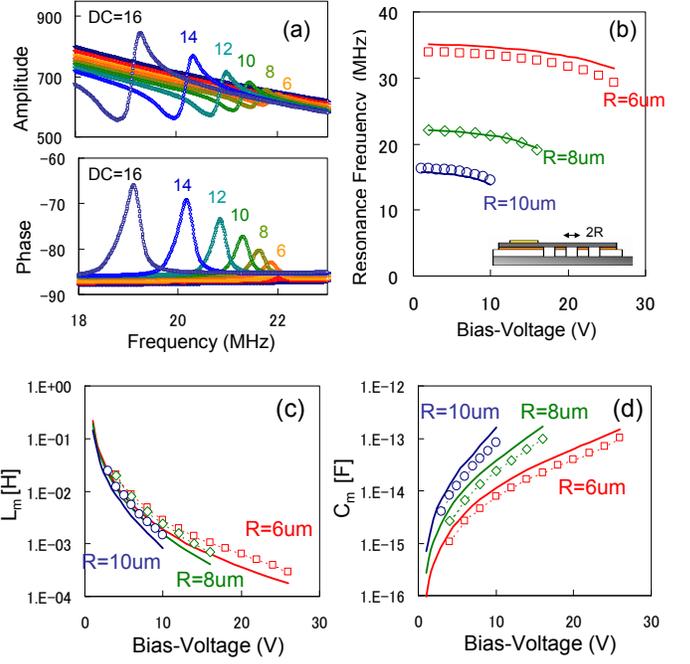


Figure 5: (a) Electrical impedance of CMUT under different DC biases. The radius of cavity is 8 μm . (b) Resonance frequency vs. DC voltage, (c) L_m vs. DC voltage, (d) C_m vs. DC voltage. Open plots are experimental results, and solid lines are simulation results obtained 1D equivalent circuit model [24].

The resonance frequency is measured in the whole 4 inch wafer. Device yield is almost 100%. Failed bits are located on the specific area, where the metal flag is temporally inserted between two wafers during wafer bonding process. The resonance frequency of 26 devices on the whole wafer is plotted on Weibull distribution as shown in Fig. 6 (a). Standard deviation of the resonance frequency is less than 1%. The distribution is not changed with different DC voltages.

In order to investigate the origin of the deviation, the amounts of deviation in cavity radius, plate thickness, and gap height which cause 1% deviation of resonance frequency are simulated using the 1D equivalent circuit model [in Fig. 6(b)]. The small dependence of the deviation of resonance frequency on DC bias in experiment indicates that the gap deviation is not major origin of resonance frequency deviation. On the other hand, 6-sigma of the silicon plate is 10 % [26], and the affected deviation of resonance frequency is calculated to be 6 %. If the distribution of resonance frequency belongs to Poisson distribution (or Gauss distribution), 6-sigma of resonance frequency is estimated to be 9 % (6%). Therefore, the main deviation is caused by the plate deviation, and the rest deviation 3% (<1%) is generated by that of cavity radius or another factor, e.g. inner, edge stress.

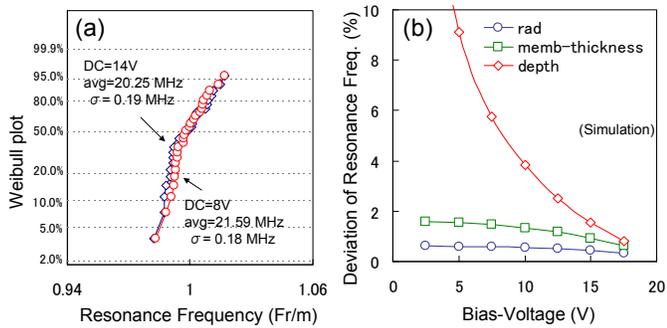


Figure 6: (a) Deviation of resonance frequency, (b) amounts of deviation in cavity radius, plate thickness, and gap height which cause 1% deviation of resonance frequency

III. SUMMARY

The surfaces with 1.6 nm RMS are successfully bonded utilizing titanium as an adhesion material, and the processes for monolithic integration of CMUTs has been developed. The electrical impedance in Air is reproducible with the simulation of 1D equivalent circuit model. The standard deviation of resonance frequency is less than 1% in the whole 4 inch wafer, and the deviation is mainly caused by that of silicon plate thickness.

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