PACKAGING OF LARGE AND LOW-PITCH SIZE 2D ULTRASONIC TRANSDUCER ARRAYS

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ABSTRACT

The successful packaging and electronics integration of large 2D array devices with small pitch-sizes, such as fully populated 2D ultrasonic transducer arrays, require a flexible, simple, and reliable integration approach. One example for such electronics integration is based on through silicon vias (TSVs) with under-bump metallization (UBM) stack for solder bumping. In this paper, we demonstrate such an approach by successfully integrating a fully populated 2D ultrasonic transducer array. Our integration is based on a previously reported TSV technology (trench-frame technology), based on trench-isolated interconnects with supporting frame. We successfully combined the trench-frame technology with a simple UBM preparation technique - electro plating or chemical plating techniques with passivation layers for UBM pad definition are not required. Our results show high shear strength (26.5 g) of the UBM, which is essential for successful flip-chip bonding. The yield of the interconnections is 100% with excellent solder-ball-height uniformity (σ = 0.9 μm). As demonstrated in this paper, this allows for a large-scale assembly of a tiled array by using an interposer. A design guideline for finer element-pitch design was developed suggesting that fusion bonding strength and the length of pillars are the main design parameters.

1. INTRODUCTION

A successful 250-μm-pitch size design based on trench-frame technology was demonstrated in [1]. However, the full strength of this technology, featuring finer pitch sizes, has not been studied yet. The key parameter for enabling large array assembly and large-scale array tiling through flip-chip bonding is an excellent uniformity of the solder height. Further, the capability of soldering on the transducer side is required for flexible packaging schemes, such as flip-chip bonding to an interposer (Fig. 1-b-3). In previous work, a post-trench UBM was formed by a 45°-tilting metal evaporation (Fig.1-a-2). The use of solder is limited to the IC (interposer) side because of the unconfined UBM pad on the transducer side. Fraunhofer IZM provides another post-trench UBM, but it is challenging to form a continuous plating seed layer by sputtering into the trench-frame structure, due to the typical negative-angle trench side-wall and over-etch induced footing on the pillars [2]. In this paper, we reported first, the process development and the test results; then the successful assembly was demonstrated and a various-pitch design guideline was provided.

2. CMUT FABRICATION AND UBM PROCESS

The capacitive micromachined ultrasonic transducer (CMUT) is composed of a silicon plate over a thin evacuated gap. Typically, a number of these plates are connected in parallel to form the top electrode. A highly conductive silicon substrate is used as bottom electrode. A contact via is created to open the buried oxide (BOX) layer for the front to backside interconnections. The bottom electrodes of array elements are separated from each other by trenches (Fig. 1a). A high topography was formed on the backside featuring the 90x90-μm wide and 255-μm tall pillars.

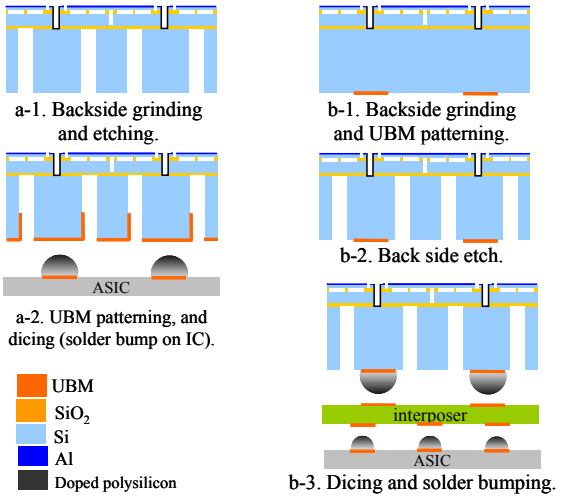


Fig. 1. Simplified backside process flow of the ultrasonic transducer array using trench-isolated interconnections on supporting-frame process. (a) The previously demonstrated post-trench UBM process [1], and (b) the new developed pre-trench UBM process that enables the uniform solder-ball heights and flexible packaging scheme.

Table I: Bump shear test results on three different metal-thickness-stacks of UBM. The UBM with 0.3μm Al/ 0.015μm Ti/ 0.3μm Ni/ 0.1μm provides strongest bump shear strength. It was also improved from the cases of brittle shear failure mode and substrate mode to the ductile mode, which provides better reliability and ease of assembly.

UBM		0.3 μm Al/ 0.015μm Ti/ 0.5 μm Ni/0.03μm Au		0.3 μm Al/ 0.015μm Ti/ 0.4 μm Ni/ 0.1μm Au		0.3 μm Al/ 0.015μm Ti/ 0.3 μm Ni/ 0.1μm Au	
Shear mode		Brittle mode 		Partial ductile mode 	Substrate mode 	Partial ductile mode 	Ductile mode 
Number of test		30	30	60		60	
Bump shear strength (g)	Mean	8.4	11.4*	24.3		26.5	
	StdDev	1.7	0.8*	5.8		1.3	

*second oven-reflow

In order to provide a simple and reliable UBM to incorporate the trench-frame interconnection technology, we developed a pre-trench UBM by e-beam evaporation of an Al/Ti/Ni/Au metal stack. The e-beam evaporated Ni provides better quality in terms of voids, which minimizes the solid-solubility induced reliability issue. The Ni thickness was chosen to be thin enough to minimize stress, yet sufficiently thick to endure double reflow of the solder.

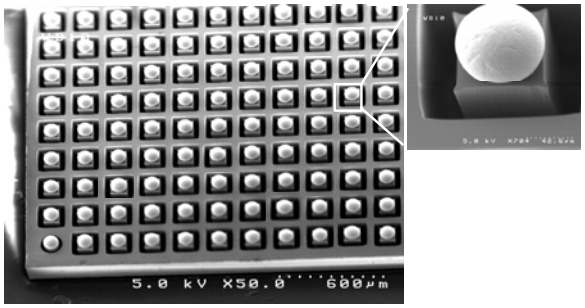


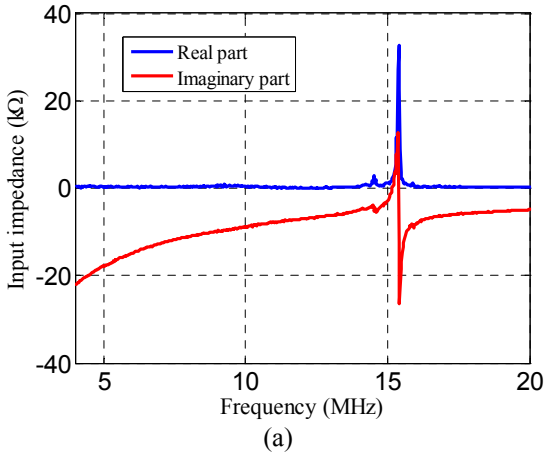
Fig. 2. SEM pictures showing solders balls on top of the trench-isolated 90x90-μm-wide and 255-μm-tall pillars with 100% yield and excellent solder-ball-height uniformity (μ = 59.7 μm, and σ = 0.9 μm).

Among various Ni/Au thicknesses (Table I), the 0.3 μm Al/ 0.015 μm Ti/ 0.3 μm Ni/ 0.1 μm Au provides the strongest bump shear strength (μ = 26.5 g) and best uniformity (σ = 1.3 g) with a preferred ductile shear failure mode. Only 0.1 μm of the Ni layer was consumed after the second oven-reflow, indicating that 0.3 μm of Ni is adequate for a double-reflow flip-chip-bonding application, which was used in our final assembly with the interposer. After solder bumping, the solder balls (Fig. 2) showed excellent height uniformity (μ = 59.7 μm, σ = 0.9 μm).

This simple UBM preparation, combined with the trench- frame technology, does not require electro plating (e.g. as used by Fraunhofer IZM, Berlin, Germany [3]) or chemical plating techniques with passivation layer for UBM pad definition (e.g. as used by Pac-Tec, Santa Clara, USA [4]).

4. TEST RESULT

The electrical input impedance was measured to determine the interconnection yield and the performance of the ultrasonic transducers after solder bumping. We used an impedance analyzer (Model 4294A, Agilent Co., Palo Alto, CA) to carry out this measurement in air (Fig. 3-a, 3-b). We serially probed the 255 signal pads through the solder-UBM-pillar-via-transducer connections on the backside of the array. The electrical input impedance was measured by sweeping the frequencies of a small AC excitation (50 mV) superimposed on top of a DC bias of 80 V (80% of the plate pull-in voltage) (Fig. 3-a). The results show 100% yield of the interconnections from all 255 elements and great uniformity of the resonant frequency of the ultrasonic transducers (Fig. 3-b).



(a)

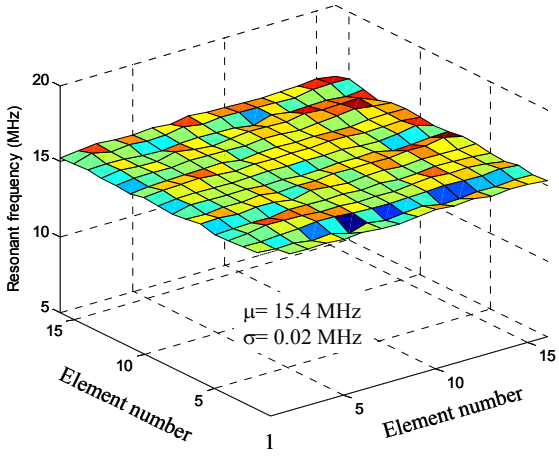


Fig. 3. (a) Electrical input impedance of one element. (b) Resonance frequency distribution across the 16x16 array. The electrical input impedance was measured by probing on the solders of one ground element and sweeping through all 255 signal elements. The results show 100% yield of the interconnections and excellent uniformity of the resonance frequency.

4. TILEABLE ARRAY ASSEMBLY

For the purpose of demonstrating large-scale tiling of the array assembly, the solder bumped devices were flip-chip bonded to an interposer (Fig. 4) [5-6]. Non-functional ASIC chips were attached on the backside of the interposer by flip-chip bonding. We successfully attached 2x12 trenched CMUT arrays on top with 1x3 ASICs on the back. The CMUT arrays were placed with 100 μm separation and it was verified that the whole module maintains the specified flatness requirement.

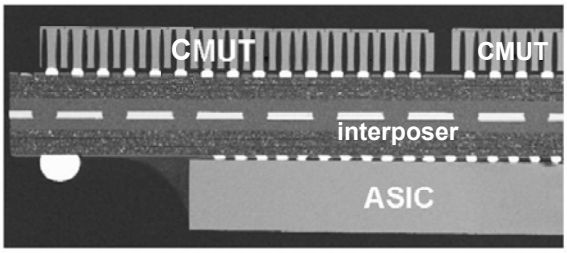


Fig. 4: Photograph of CMUT devices flip-chip bonded to the topside of a laminate interposer.

5. DESIGN GUIDELINE

We demonstrated the 185-μm tall 90x90-μm wide pillar could endure the interposer assembly process. For finer element pitch sizes and wafer thicknesses, a design guideline was developed by using a beam theory calculation and finite element analysis (FEA). First, we calculated the induced maximum tensile and shear stress at the bottom of the signal pillar under the bump-shear force acting on the top of the pillar (Fig. 5-a). The pillar bottom reflects the Si-BOX interface or the interface within the BOX layer. The analysis predicted less than 4.5 g of bump shear force can result in a tensile stress level of tens of MPa, which reflects the fusion bonding strength [7] and the tensile strength of thermal-grown silicon dioxide. The FEA result shows the same stress level thus agrees with the calculation (Fig. 5-b).

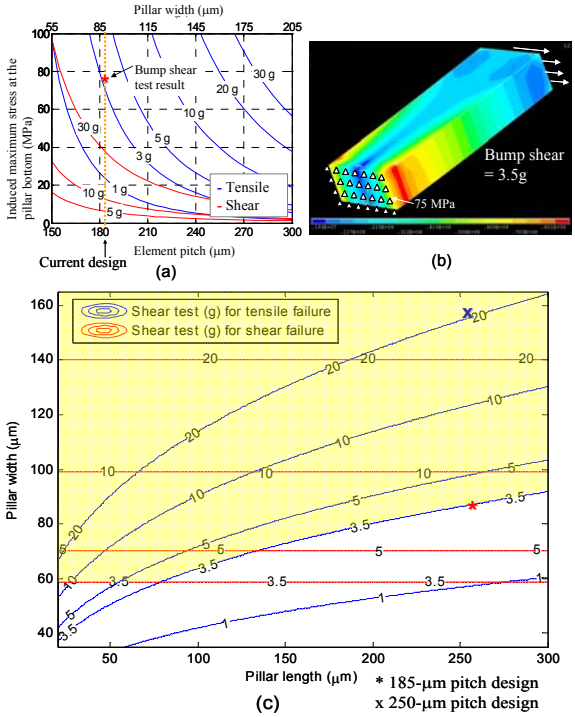


Fig. 5. (a) Beam theory calculated induced maximum tensile and shear stress at the bottom of the signal pillar under the bump-shear force acting on the top of the pillar. (b) Finite element analysis agrees with the beam theory calculation with only 6.7% error. (c) Design guideline for pitch (pillar width) and substrate thickness (pillar length) with experimental-determined fusion-bonding strength. The tensile fusion bonding strength was based on the bump-shear test of 3.5 g results with the beam theory calculation. The yellow region indicates the verified safe zone for various pillar width and length designs.

We further verified this analysis by a shear strength test on the solder-bump-pillar (Fig. 6-a). Five sample data all show between 3.4 g and 3.6 g (μ = 3.5 g, σ = 0.1 g), which agree with our prediction. The post-failure patterns (Fig. 6-b, 6-c), showing the remaining oxide on the bottom of the trench, indicated that the failure is through the BOX-Si interface and/or the BOX layer of the silicon on insulator (SOI) wafer. For even finer pitch designs, the fusion bonding

adhesion should be enhanced, and/or the pillar length should be shortened.

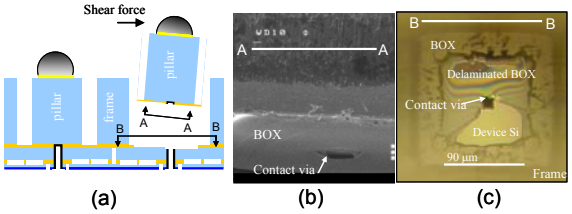


Fig. 6. (a) Cartoon showing the bump-shear test on a signal pillar. (b) SEM on the bottom of a post-shear-failure pillar showing the presence of a BOX layer. The shear failure interface is through the Si-BOX interface but not the Si pillar. (c). Microscopic optical picture shows the bottom of the trench with the fringing patterns within the 90x90 µm square. The fringing pattern indicates the delaminated BOX from device Si layer.

6. CONCLUSION

The initial work on a packaging and electronics integration method of large-scale tile able 2D array devices with small pitch-sizes has been demonstrated. A pre-trench UBM, by e-beam evaporating Al/Ti/Ni/Au metal stacks, was developed to incorporate to the trench-frame interconnect technology. This simple UBM was proved to provide good bump shear strength and excellent solder ball height uniformity along with a preferred ductile shear failure mode. Test results show 100% yield of the interconnections and great integration uniformity as indicated by the air resonance performance over 255 transducer elements.

We also demonstrated a tile able module assembly and the CMUTs-interposer-ASICs sandwich by a complete flip-chip attach. Future work includes the assembly of large-scale functional CMUT chips by tiling and the acoustic tests on such assemblies.

A design guideline for various element-pitch and wafer-thickness based on trench-frame technology was developed. In the current design, the 185-µm tall 90x90-µm wide pillar can endure the interposer assembly process. The bump-shear test shows that the failure is through the Si-Box interface and/or the BOX layer. For designs with smaller pitch, the fusion bonding adhesion should be enhanced (if possible), and/or the pillar length should be shortened.

ACKNOWLEDGEMENTS

The project described was supported by Grant Number 1R01CA1152677 from the National Cancer Institute. Its contents are solely the responsibility of the authors and do not necessarily represent the official views of the National Cancer Institute or NIH.

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