

FLEXIBLE TRANSDUCER ARRAYS WITH THROUGH-WAFER ELECTRICAL INTERCONNECTS BASED ON TRENCH REFILLING WITH PDMS

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ABSTRACT

This paper reports on a method to fabricate flexible one-dimensional (1D) and two-dimensional (2D) micromachined transducer arrays that are electrically connected to flip-chip bond pads on the back side of the array. In our case, the transducers are capacitive micromachined ultrasonic transducers (CMUT) intended for medical ultrasound imaging. For ultrasound imaging, flexible arrays conform to the body part being imaged. Flexible arrays are also desired for certain catheter and fixed-focus array geometries. Electrical connection to bond pads on the back side of the array is provided for flip-chip bonding to an integrated circuit or flexible PCB. The arrays are made flexible by etching through-wafer trenches and filling the trenches with polydimethylsiloxane (PDMS). The flexibility of the substrate is demonstrated by wrapping it around a needle tip with a radius of 650 μm (French catheter size of 4).

1. INTRODUCTION

In recent years, researchers have demonstrated flexible silicon structures based on polymer-coated trenches [1]. Polymer-based structures have also been shown as a flexible carrier for MEMS sensors by different research groups [2, 3]. Here we use PDMS to refill through-wafer trenches and incorporate a means of routing electrical signals on a 2D array to the back side of the silicon wafer.

Mechanically flexible and biocompatible PDMS is well-suited as a coating material for medical ultrasound transducers. PDMS typically has a high electric break down field (~ 20 kV/mm), which insures good insulation between the device and the living tissue. The acoustic impedance of PDMS is close to water, and efficient energy transfer between the transducer and the medium (water) through the PDMS layer is possible. Moreover, PDMS is thermally stable at relatively high temperatures (>200 $^{\circ}\text{C}$), making it compatible with solder-based flip-chip bonding. Benefits of flip-chip bonding as a method to attach MEMS devices to the driving electronic circuits include independent device optimizations for the respective parts, broader processing conditions, increased yield and lower costs. When used to refill through-wafer trenches, PDMS provides mechanical linkage between neighboring silicon pillars. The silicon pillars act as the through-wafer

electrical interconnects for the array elements in a 2D array. Wafers with patches of such flexible regions can be handled like regular silicon wafers.

2. DESIGN

The CMUT is composed of membranes over shallow vacuum cavities. Typically, the membrane thickness is in the order of 1-10 μm , and the cavity is less than a micron deep. A number of these membranes are connected in parallel and form the top electrode. In the trench-isolated CMUTs, highly conductive silicon substrate is used to form the bottom electrode. The bottom electrodes of array elements are separated from each other by the through-wafer trenches. Fig. 1 illustrates the device operation concept.

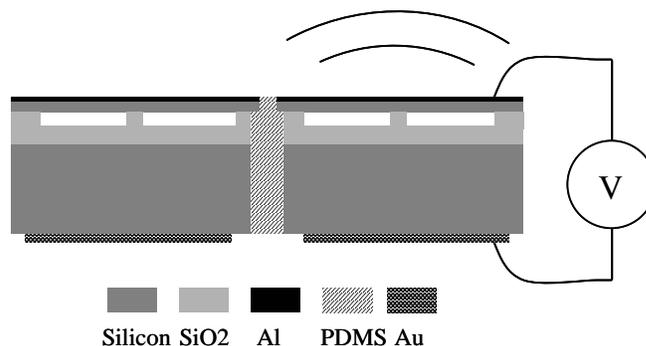


Figure 1: Cross-sectional schematic of two flexible CMUT array elements. One element is excited to transmit ultrasound waves into the surrounding medium.

The CMUT has a 250- μm element pitch. Each element consists of eight rectangular membranes that are 1.83- μm thick, 40- μm wide and 140- μm long. The cavity height is 0.15 μm , and the oxide insulation layer is 0.3- μm thick, designed according to the operating voltage requirements. Compared with conventional trench-isolated CMUTs [4], the CMUT devices reported in this paper feature PDMS-refilled isolation trenches to enhance mechanical flexibility and ease of handling.

3. FLEXIBLE SILICON SUBSTRATE

Fig. 2 shows the 2D array fabrication process used to demonstrate flexible silicon substrate by trench refilling with PDMS. The width of the silicon trenches varies from $8\ \mu\text{m}$ to $50\ \mu\text{m}$, and the depth varies from $50\ \mu\text{m}$ to $200\ \mu\text{m}$. The pitch of silicon pillars is $250\ \mu\text{m}$. Each 2D array consists of 16 by 16 elements, and measures 4 mm by 4 mm on the sides. After curing the PMDS on a hot plate, the wafer back side is etched to the bottom of refilled trenches.

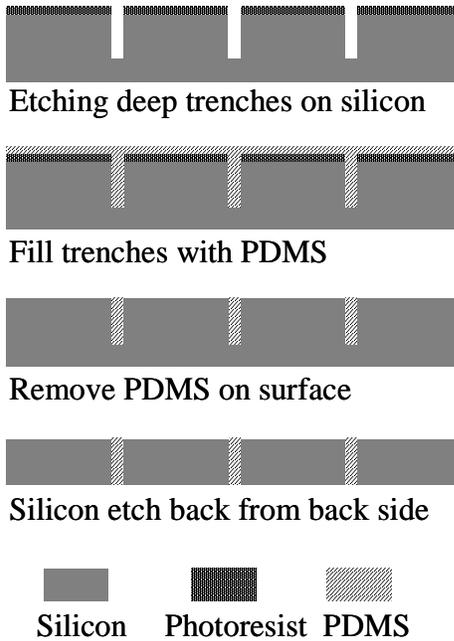


Figure 2: Fabrication process demonstrating flexible silicon substrate by through-wafer trench-refilling of PDMS.

After fabrication, the wafer can still be handled like a regular silicon wafer. To test the flexibility of the trench-isolated silicon pillars, a 2D array with a $200\text{-}\mu\text{m}$ thick substrate was bent by tweezers to conformally cover a needle tip with a radius of $650\ \mu\text{m}$, emulating a side-viewing catheter tip for intravascular ultrasound (IVUS) applications, as shown in Fig. 3 (a). Fig. 3 (b) shows that the silicon substrate returned to its original shape after the bending force was removed. Fig. 3 (c) and (d) illustrate that such an array stretches when pushed by a needle tip in the center, and returns to the original shape after the removal of the needle tip.

The flexible substrates were heated to $220\ ^\circ\text{C}$ on a hot plate for 5 minutes, to emulate the thermal reflow process condition for Sn/Pb eutectic flip-chip bonding used to

integrate CMUT arrays to front-end IC. After the thermal cycle, the substrate retained the same flexibility.

We tried three different kinds of Dow Corning PDMS to refill the trenches: Sylgard 182, Sygard 184 and 1-4105. The resulting substrates showed similar flexibility from these three PDMS.

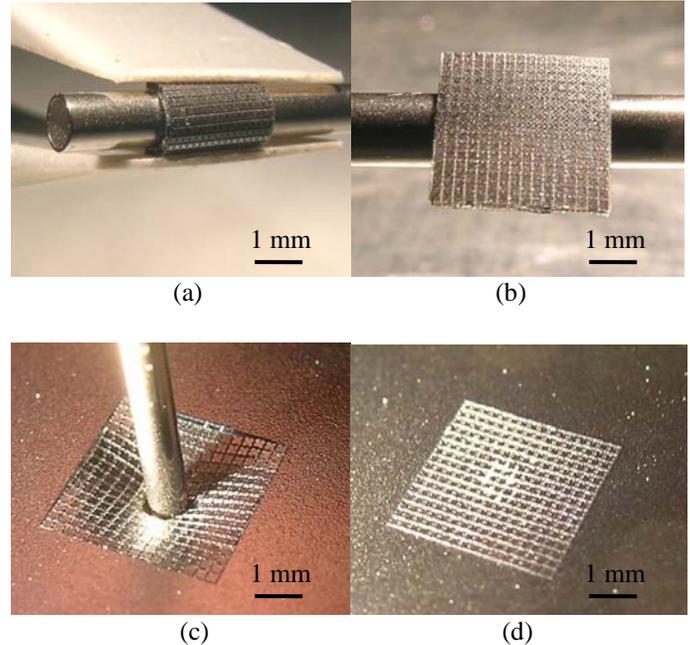


Figure 3: Flexible silicon substrate realized by refilling through-wafer trenches with PDMS.

4. CMUT FABRICATION

Fig. 4 shows the fabrication steps to incorporate CMUT elements onto a flexible silicon substrate. First, the CMUT cavities are defined on the front side of a prime silicon wafer by oxidation and etching. Deep trenches are then patterned and etched into the silicon substrate using deep reactive ion etching (DRIE). These trenches have varying widths of $6\ \mu\text{m}$ to $20\ \mu\text{m}$, and are about $150\text{-}\mu\text{m}$ deep. The wafer is then fusion bonded to a silicon-on-insulator (SOI) wafer and annealed at $1100\ ^\circ\text{C}$ for one hour. The silicon handle on the SOI wafer is removed in heated tetramethylammonium hydroxide (TMAH) solution, leaving only the $1.83\text{-}\mu\text{m}$ thick silicon device layer as the CMUT membrane. The membrane is metallized with a $0.4\text{-}\mu\text{m}$ thick layer of aluminum to form the common electrode. Holes with diameters of $4\ \mu\text{m}$ to $10\ \mu\text{m}$ are then etched in the membrane regions that overlap the trench areas to allow the PDMS to fill into the trenches. After dispensing PDMS, the wafer is put into vacuum for two minutes to allow air to be evacuated from the trenches. This

step is repeated for three times to ensure good PDMS filling in the trenches. The PDMS thickness is controlled by the subsequent spinning step. Using Dow Corning 1-4105 PDMS, a 30- μm thick layer is obtained by spinning at 500 rpm for one minute. The PDMS is cured on a hot plate at 110 $^{\circ}\text{C}$ for two hours. The PDMS layer on the CMUT membranes provides a bio-compatible coating for the CMUT. After etching the silicon substrate from the back side, the array elements are electrically isolated from one another, but mechanically linked by the PDMS in the trenches.

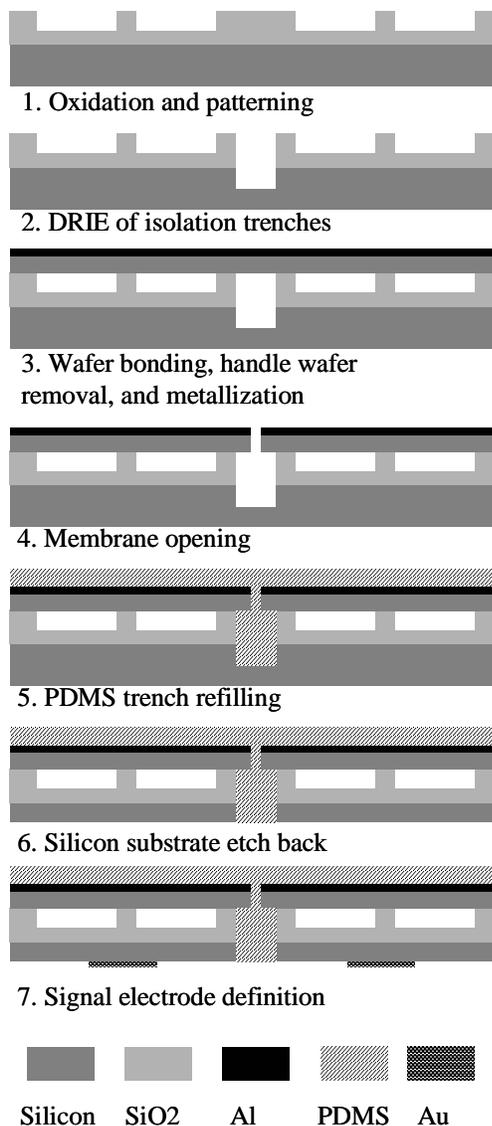


Figure 4: Simplified schematic diagrams of modified process flow to incorporate CMUT elements on flexible silicon substrate.

Fig. 5 (a) shows the top view of the CMUT membranes corresponding to the step 6 in Fig. 4. Magnified view of the holes on the membranes used to fill the trenches beneath with PDMS is shown in Fig. 5 (b). The PDMS was able to fully fill the trenches, as shown in the device cross-section in Fig. 5 (c).

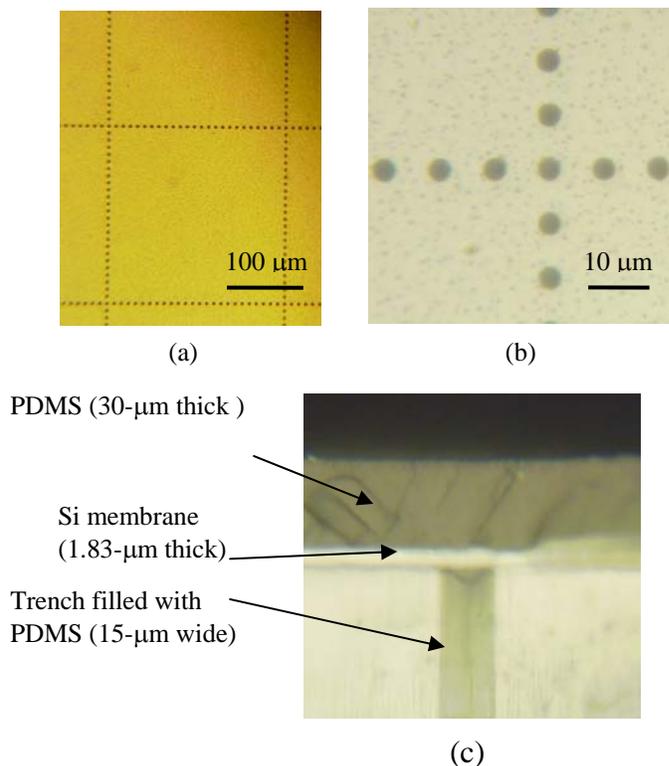


Figure 5: Photographs of a fabricated Device.

5. TEST RESULTS

The CMUT was biased at different DC voltages and the device capacitance was then measured using a network analyzer (Model 8751, Hewlett-Packard Company, Palo Alto, CA). Fig. 6 (a) shows the capacitance as a function of bias voltage. The capacitance increased with the bias voltage due to the reduced cavity height as a result of the electrostatic force between the membrane and the substrate. A parallel plate model predicts a device capacitance of about 2 pF. The measured capacitance is close to the predicted value. The difference can be attributed to the parasitic capacitance and the parameter uncertainties, such as gap height and insulation layer thickness, caused by processing.

The resonant frequency in air was also extracted from the measurements made using the network analyzer. Fig. 6 (b) shows the dependency of the open circuit resonant frequency, where the real part of the input impedance is maximal, on the

DC bias voltage. The predicted resonant frequency based on the equivalent circuit model for such a CMUT device without PDMS coating is around 9.3 MHz. The decreased resonant frequency is attributed to mass loading of the PDMS on the membrane.

The collapse voltage of the CMUT membranes was measured to be 120 volts. At this voltage no DC leakage current was observed, proving good insulation provided by the PDMS filling material in the trenches.

These arrays bend when pushed in the center. However, cracks will form in the silicon membranes that overlap the trenches, and propagate to the device areas. Thin silicon ribbons have been used as flexible interconnects for MEMS systems [5]. Such ribbons will be incorporated into future designs to replace the whole membranes in the trench area to reduce the probability of cracking.

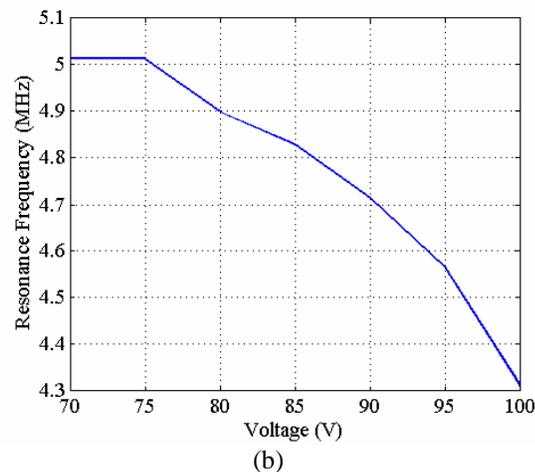
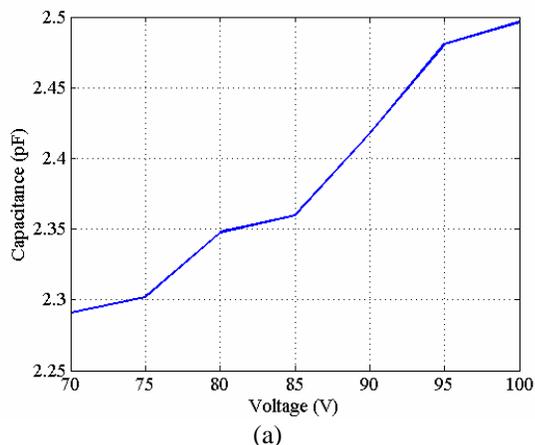


Figure 4: (a) CMUT device capacitance as a function of DC bias voltage; (b) resonant frequency as a function of DC bias voltage.

6. CONCLUSION

Flexible silicon substrates based on through-wafer trench refilling of PDMS have been demonstrated. The finished device wafers can be handled like regular wafers. These substrates can be wrapped around catheter tips with a radius of 650 μm or less, and are potentially useful for IVUS applications. The PDMS was also shown to be able to sustain high temperatures used in the flip-chip bonding process for integrating the CMUT to the front-end IC.

We also demonstrated a fabrication process to incorporate CMUTs onto the flexible silicon substrate. Through-wafer electrical interconnection was realized by this process. The CMUT device was tested to be active by capacitance and resonant frequency measurements. The PDMS provided sufficient electrical insulation between the array elements and ground.

In the current design, the flexibility of the CMUT array is limited by the continuous silicon membranes above the trenches. In future designs, narrow stripes of silicon can be used to connect the neighboring elements to increase the device flexibility.

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