Characterization of Fabrication Related Gap-Height Variations in Capacitive Micromachined Ultrasonic Transducers

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***Abstract* – The gap-height directly affects the static operation point of the CMUT which in turn affects the receive sensitivity and the total possible output pressure. In this paper we report on the characterization of fabrication related gap-height variations in CMUTs. The CMUTs under investigation using the sacrificial release process were found to have lower collapse voltage, smaller maximal membrane deflection and missing pull-in behavior as compared to theory. The in-cavity deposition was examined by SEM and the surface topography on the bottom side of the gap by AFM. The AFM measurements were evaluated for devices with and without in-cavity-deposition as well as devices fabricated with doped polysilicon film or doped bulk silicon for the bottom electrode. A methodology to determine the contribution of each layer in the fabrication process to surface roughness is presented. Our results show that surface roughness reduces the actual gap-height, and the polysilicon layer is the main contributor.**

***Key words* – CMUT; gap-height; surface roughness; in-cavity deposition; sealing; bottom electrode; doped polysilicon**

I. BACKGROUND AND MOTIVATION

CMUTs are a promising alternative to the piezoelectric transducers for medical imaging because of their fabrication flexibility and improved performance, including wide bandwidth and efficient transmission in immersion. To design CMUTs arrays for medical imaging, we optimize gap height, membrane radius, and membrane thickness for the optimum total acoustic output pressure, transmission efficiency, and reception sensitivity. All of those are strong functions of gap-height (Table 1).

Table I. Performance index as functions of gap-height

Performance Index	Function of gap
Acoustic output pressure	$\propto$ gap
Transmission efficiency	$\propto 1/\text{gap}^2$
Reception sensitivity	$\propto 1/\text{gap}^2$

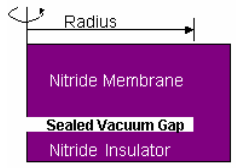
For high frequency designs, a small gap height, as small as 50nm, is needed to maintain a reasonable collapse voltage. Fabricating such a small gap with the sacrificial release process is very challenging. Any deviation from the expected gap-height could lead to large changes in performance.

II. MATERIALS AND METHODS

For our desired 2D structure, we choose the sacrificial release process because through-wafer-vias, a well established technology for the electronics integration, can be easily incorporated into the process. With a 10MHz desired center frequency, a gap of 120nm was chosen to maintain a reasonable collapse voltage. The transducer's specifications are given in Table II.

Table II. Design parameters and values

Design parameter	Target value
Center frequency	10MHz
Radius	15.5µm
Membrane thickness	650nm
Gap height	120nm
Insulator thickness	180nm



To investigate the pull-in behavior and compare with our models, we measured the frequency response of the transducer and also the deflection of the membrane under applied DC voltage. We measured the frequency response using a vector network analyzer (HP 8751A) under applied DC voltage (SRS PS 310 high voltage power supply, Stanford, CA). The static deflection was also measured using a white light interferometer (Zygo NewView 2000) under applied voltage. The static deflection not only enabled us to see the membrane pull-in but also the total maximum deflection that should be equivalent to the gap height.

We verified that our process produced the desired

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gap-height by using a scanning electron microscope (FEI XL30 Sirion SEM) to view the cross-section of a cell. The gap-height was confirmed by measuring the height at the edge of the cell. This is because other points at the center of the membrane are deflected downwards from stress in the nitride, so only the edge is the correct measurement of the gap-height. A SEM measurement was also performed to view the surface roughness of the bottom side of the gap by peeling off the CMUT membrane.

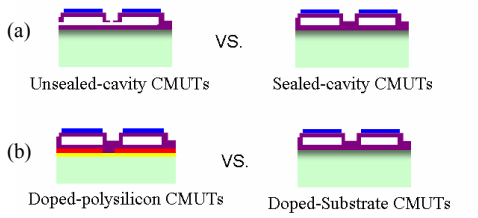

Fig. 1: The comparison of the surface roughness from the bottom side of the gap between (a) The CMUTs with and without sealing, and (b) The CMUT with doped polysilicon and thermal oxide and the one with doped substrate

In order to identify the source of the surface roughness, we used Digital Instruments Nanoscope 3000 Atomic Force Microscope (AFM) to compare devices with and without in-cavity-deposition as well as devices with heavily doped polysilicon film versus heavily doped bulk silicon as bottom electrode (Fig. 1).

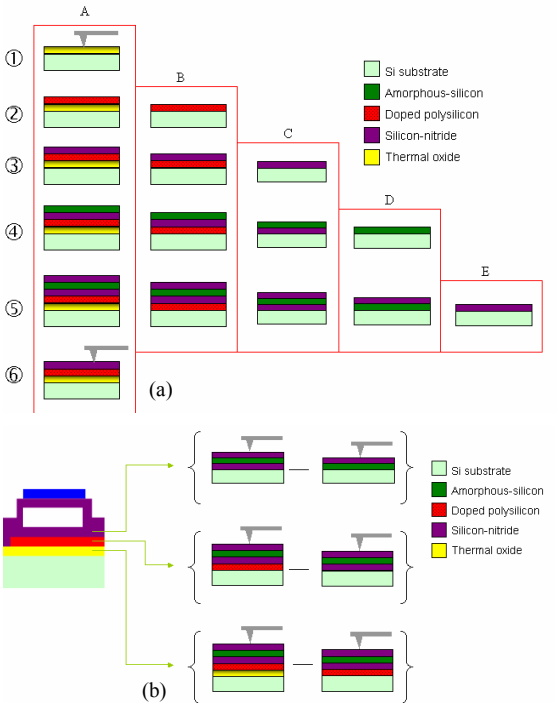

Fig. 2: The methodology to quantify the roughness of each layer

The results of the AFM on the actual device motivated us to do a more systematic study using the AFM to measure the surface topography of different material layers at different points in the process (Fig. 2). Starting from five wafers, every wafer starts from each offset process step. This approach enabled us to measure the roughness of individually new-deposited layers (wafer A1, B2, C3, D4, and E5), and also to monitor the surface roughness change through the real process run (wafer A1~A6).

In addition, the contribution of surface roughness from each layer is available from the comparison as shown in Fig. 2(b). Since the roughness is the combination of the material itself in association with the experienced thermal cycles, the surface roughness of interest has to include the effects of the neighboring layers during thermal cycling. It is difficult to etch back layer by layer without altering the surface topography, so we compared the difference of the results between the case with and without the layer of interest.

III. RESULTS AND DISCUSSION

A. Static deflection and Impedance measurements

Static deflection measurements and the frequency response were used to verify the response of our designed membrane with the model. We expected to see a pull-in behavior around 65V and a deflection of 120nm. Instead, we found that the pull-in behaviors were missing and the deflection saturated at 80nm instead of 120nm of the gap-height (Fig. 3), which motivated us to study the gap-height variations.

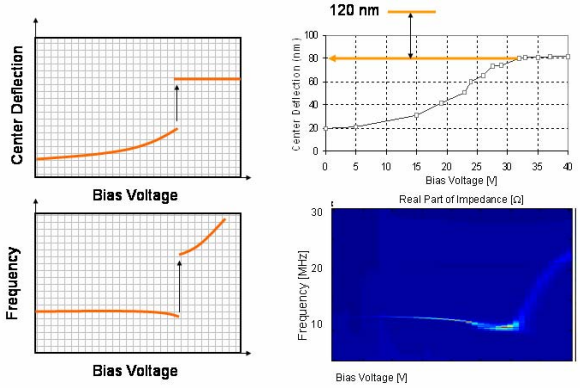

Fig. 3: Behavior of center deflection versus DC bias and real part of input impedance versus DC bias: (a) Theoretical part, and (b). Measurements part.

B. SEM measurements

The gap height from the edge of the cell was measured to be 120±10nm from our SEM picture (Fig. 4a), which is very close to our design. The measurement showed that the total in-cavity deposition was well controlled by the reduced-height sealing channel.

We further used the SEM to view the bottom side of the gap (Fig. 4b) and saw a roughness that was the same order as gap-height, which may account for the gap-height variations.

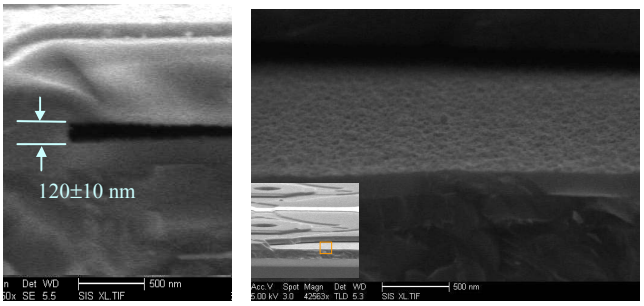

Fig. 4: (a) SEM photograph (cross-section) of one CMUT cell showing the gap-height, and (b) SEM photograph of surface roughness from the bottom side of the gap

C-1. AFM comparisons of various CMUTs

There are two sources of the roughness at the bottom of the cavity: in-cavity deposition and also individual roughness of various layers.

We first compared the surface roughness of an unsealed and sealed cavity and found very close surface roughness of 3.8nm and 3.9nm RMS (Fig. 1a), respectively. This indicates the sealant does not contribute to the surface roughness. Next, we investigated whether roughness of the underlying layers contributed to the roughness by comparing the cases in Fig. 1(b). CMUTs with doped polysilicon and underlying thermal oxide showed 9.5nm RMS, which is much higher than 3.9nm RMS of CMUTs with doped bulk silicon substrate. It means the cumulative roughness from underlying layers significantly contributes to gap-height variation.

C-2. AFM differential comparisons of a process mimicking the real fabrication run

Given that the underlying layers contributed to the surface roughness, we investigated roughnesses of each individual deposited layer as well as combinations of layers through thermal cycles in the process. First we investigated the contribution of individual layers (Table III: wafer A-1a, B-2a, C-3, D-4, and E-5). We found that the polysilicon produces the most roughness, 108±24nm, which is 16-120 times greater than the roughness of any other individual layer.

Table III. RMS surface roughness measured by AFM

	Process step	Temp. Time	A	B	C	D	E
0	Prime wafer	-	0.1 nm	0.1 nm	0.1 nm	0.1 nm	0.1 nm
1a	Thermal oxide	1000°C 4h.50m	0.2 nm	-	-	-	-
1b	Thermal cycles	-	-	-	-	-	-
1c	Etch-backh to the oxide	-	3.0 nm	-	-	-	-
2a	LPCVD polysilicon	620°C 1h.20m	17.5 nm	23.9 nm	-	-	-
2b	P diffusion doping	900°C 1h.30m	10.4 nm	13.9 nm	-	-	-
3	LPCVD low-stress nitride	785°C 1h	9.7 nm	11.8 nm	1.2 nm	-	-
4	LPCVD amorphous silicon	560°C 57m	8.0 nm	10.5 nm	1.4 nm	0.3 nm	-
5	LPCVD low-stress nitride	785°C 5h.05m	8.4 nm	9.9 nm	1.7 nm	1.5 nm	1.5 nm
6	TMAH wet-release	-	9.2 nm	-	-	-	-

We next investigated the roughness of successive layers during processing (Table III: wafer A0~A6). A-1a shows that the oxide layer itself does not add roughness, and then the surface became rougher with 3nm RMS (Fig. 5) in A-1c. The reason is that the oxide has glass transition temperature is between 900°C to 1100°C [3]. The oxide was softened due to the much lower viscosity at 1000°C. Meanwhile, the grain growth of the polysilicon layer punctures the oxide. As a consequence, the oxide is imprinted by polysilicon during high temperature and left with a higher roughness.

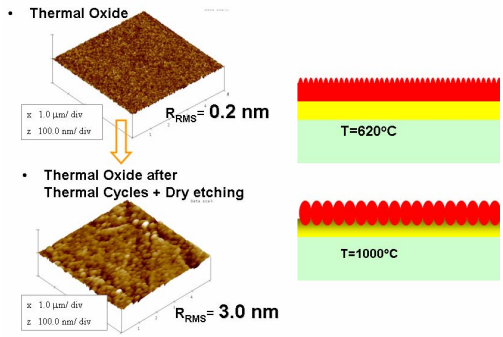

Fig. 5: Thermal Oxide is roughened due to imprinting by overlying polysilicon layer

In Table III: A-2a, the deposition of LPCVD polysilicon and doping with phosphorus increases surface roughness from 3 to 17.5nm RMS. It is the largest roughness rise through the whole process. In contrast, the largest reduction

of surface roughness occurred after the doping step, which reduced the value from 17.5nm RMS to 10.4nm RMS (Table III: A-2b). This reduction may be a result of the 900°C annealing used to dope the polysilicon, which not only joined and enlarged the grain size in x-y direction but also relaxed the high surface energy from columnar grain structure [2] to the typical hemisphere grain shape (Fig. 6) [4].

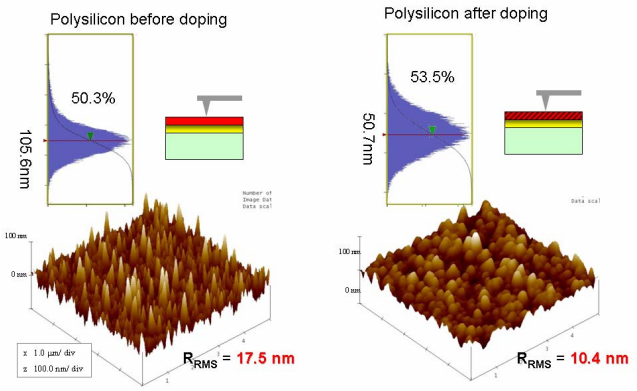

Fig. 6: Doping reduces surface roughness of polysilicon

The relative smooth nitride layer was grown after the doping, which provide a conformal deposition and results in a smoother surface from 10.4nm RMS to 9.7nm RMS [table III: A-3]. Through steps A-4~6, the nitride shows a surface roughness value of 9.2nm RMS, which is very close to our measurement from actual devices.

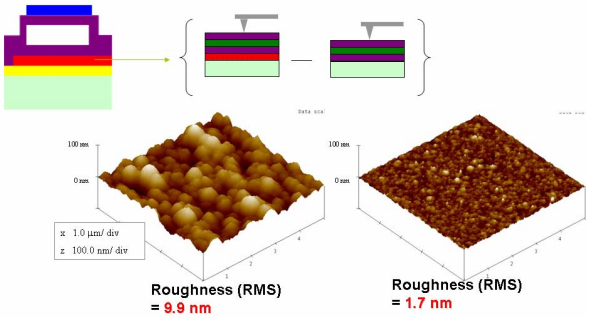

Fig. 7: Roughness contributed from doped polysilicon

C-3. Roughness contribution from various layers

In order to see the contribution of surface roughness from each layer, we compared three pairs of wafers with and without the layer of nitride, thermal oxide and polysilicon. Both of the cases with and without nitride and oxide (Fig. 4b-I, III), were similar in surface roughness, measuring 1.7nm RMS versus 1.5nm RMS and 8.4nm RMS versus 9.9nm RMS (Table III: C-5 vs. D-5 and A-5 vs. B-5), respectively. Compared to the case shown in figure 4b-II, the roughness 9.9nm RMS with polysilicon layer compared to 1.7nm RMS without polysilicon (Table III: B5 vs. C5) proves that the doped polysilicon layer is the main contributor to the final surface roughness.

IV. CONCLUSIONS

The characterization of fabrication related gap-height variations in CMUTs was studied in this paper. Our results show that the surface roughness reduces the actual gap-height, and the polysilicon is the layer most responsible for the increased surface roughness. In the future, surface roughness should be accounted for in small gap designs if the nitride sacrificial release method is used. Otherwise, an SOI wafer bonding for thin gap devices should be used.

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