EXTENDED INSULATION LAYER STRUCTURE FOR CMUTS

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***Abstract*—Electrostatic transducers require an electrically insulating structure between their electrodes. In state-of-the-art transducers, such as capacitive (micromachined) ultrasonic transducers (CUTs, CMUTs), this insulating structure is the main limiting factor in terms of device reliability (electrical breakdown, parasitic charging effects) and device performance (thin gap devices with low parasitic capacitance). We present a configuration, based on an extended insulation layer structure, which addresses all of these issues. A deep-trench-oxidation technique is used, that allows the fabrication of a released thermally-grown silicon dioxide structure, which can be more than 30 μm deep extended into the substrate. Preliminary measurement results from a CUT, featuring a back plate with such a deep extended insulation layer structure, are presented. The approach of using an extended insulation layer structure not only can improve the present CUT and CMUT technology in terms of reliability and performance, it also opens the door to high temperature applications of various types of electrostatic transducers.**

I. INTRODUCTION

Micromachining techniques have developed over the last few decades enabling precise control over structures on a nanometer scale. This progress was successfully employed to realize capacitive micromachined ultrasonic transducers (CMUTs) with small electrode separations, characterized by high electric field strengths in the gap. Unfortunately, in state-of-the-art CMUT cells, the desire for small electrode separations is fulfilled by using thin insulation layers at both the gap and post region [Fig. 1(a)]. The drawback of this approach is threefold: reliability issues due to electrical breakdown; high electric field strengths in the insulation layer resulting in charging problems; and a large parasitic device capacitance. In this paper we present an extended insulation layer structure that addresses all three issues. It can be used for CMUTs, fabricated primarily via direct wafer bonding technique, and for the fabrication of back plates for CUTs.

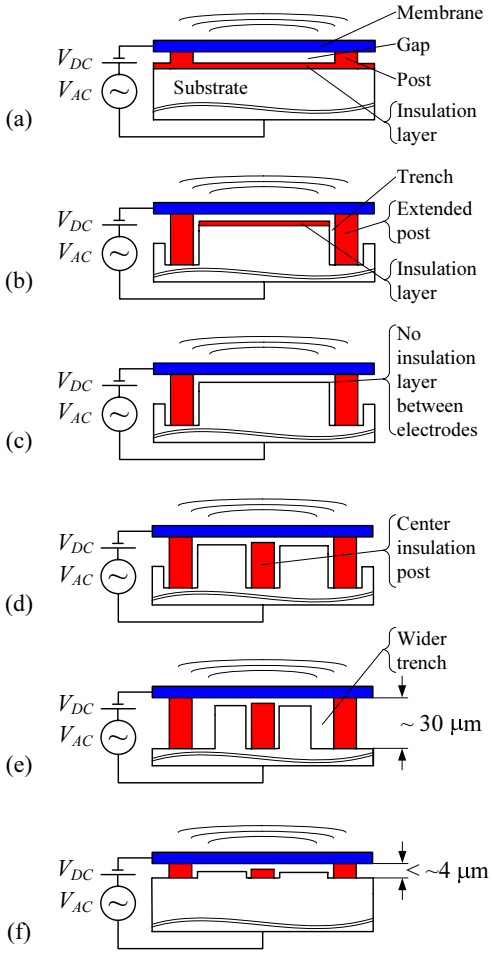

Fig. 1. Schematic of a traditional capacitive ultrasonic transducer cell (a) in direct comparison to various improved cell configurations (b)-(f). Red is an insulating material, such as silicon dioxide, blue is preferentially conductive, such as doped silicon or silicon carbide (for CMUT, top electrode is then optional) or a metal foil (for CUT). If the membrane (blue) is non-conductive (*e.g.* silicon nitride, nanocrystalline diamond film) then a top electrode is required (not shown).

II. PROBLEM STATEMENT AND SOLUTIONS

The height of the insulation layer in a cell configuration, as shown in Fig. 1(a), is a limiting design factor in terms of the electrical voltage or the temperature, or both, that can be applied to the device. There are three

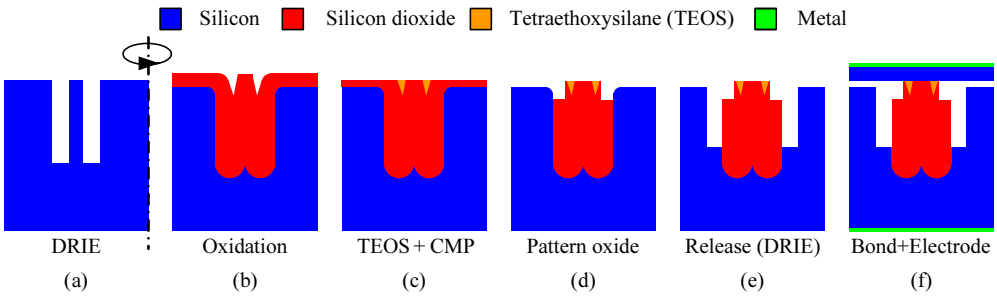

Fig. 2. Key steps of the fabrication process to realize a released $\sim 4 \ldots 30$ μm-deep thermally-grown S_iO_2 insulation structure. Each figure (a-f) shows the cross section of a circular shaped structure.

main mechanisms that need to be considered:

First, if the insulation layer is stressed by large electric field strengths, the lifetime of the device is ended or reduced due to electrical breakdown. For common insulation materials used in microelectronics and MEMs industry, such as silicon dioxide or silicon nitride, the electrical breakdown voltage reduces with increasing temperature [1].

Second, high electric field strengths in the insulation layer, or the combination of both high electric field strengths and high temperatures (BT-stress [2]), can result in parasitic charging effects in the insulation layer. For example, in silicon dioxide, mainly positively charged alkali ions [3] form a charge layer that degrades the electric field strength inside the gap and thus the device performance. The mobility of these charges strongly depends on temperature [2], which makes the charging problem even more severe at elevated temperatures.

Third, due to the higher dielectric constant of the insulation material of the insulation layer compared to vacuum or air inside the gap, the insulation post [Fig. 1(a)] contributes significantly in terms of parasitic device capacitance.

The cell configurations shown in Figs. 1(b)-(f) address these issues:

The insulation posts can be extended into the substrate to increase the electrical breakdown voltage and to reduce the parasitic device capacitance significantly [Fig. 1(b)]. This configuration features a better breakdown performance only within the pull-in point of the membrane, *i.e.* non-collapsed membrane, and it does not address the charging issue.

However, it enables a configuration where the insulation layer between the electrodes can be removed completely [Fig. 1(c)], which eliminates the charging problems. The advantage of this solution, compared to [4], is that the extended posts have a reduced surface conductivity. This lowers the likelihood of an extrinsic breakdown. However, the device still can not be operated beyond pull-in point.

To eliminate this last drawback, we realized a configuration that features an extended center post [Fig. 1(d)]. Not only this configuration features a better electrical breakdown performance within and beyond pull-in point operation, it also eliminates parasitic charging effects and it has a reduced parasitic device capacitance. This is our prime cell configuration featuring an extended insulation layer to realize CUTs and CMUTs for various applications.

In general, the effort required to realize such a cell configuration will depend on the height of the extended posts. For example, if thermal-grown silicon dioxide is considered as insulation layer material, then a configuration as shown in [Fig. 1(f)] can be realized easily. However, if deep thermally-grown silicon dioxide posts are desired ($\sim 4 \ldots 30$ μm), then more effort in terms of fabrication is required. This is outlined in Fig. 1(e), which shows a cell configuration with a wider trench for further optimization in terms of parasitic capacitance. This idea can be used instead of half-metallized CMUT electrodes, which are more sensitive in terms of thermal-induced stress effects than full metallized electrodes [5].

In case that these configurations [Figs. 1(d)-(f)] are used for non-sealed CMUTs or back plates for CUTs, then electrical breakdown phenomena in air at micron separations need to be considered [6]. Besides the general advantages of these cell configurations for almost every application of CMUTs, we aim to use the configuration from Fig. 1(d) to realize a high-temperature ultrasonic transducer technology, *i.e.* high-temperature capacitive micromachined ultrasonic transducers (HTCMUTs) and high-temperature capacitive ultrasonic transducers (HTCUTs). Therefore, we fabricated the insulation structure with an extension depth of more than

30 μm to account for the reduced electrical breakdown voltages of silicon dioxide at elevated temperatures.

III. Fabrication of Deep Oxide Posts

The developed fabrication process for the insulation layer structure is an extension of the well-known technique of thermally oxidizing multiple high-aspect-ratio trenches, formed via deep reactive ion etching (DRIE) [7], [8]. Compared to this state-of-the-art technique, our fabrication process (Fig. 2) is distinguished by having the following two main features: Instead of multiple trenches, we only use two circular concentric trenches for each structure and we partially release the structure. Further, we succeeded to bond another wafer to this released structure using direct wafer bonding technique.

After etching the circular shaped trenches via DRIE [Fig. 2(a)], the wafer is oxidized until the silicon ring between the trenches is transformed in a solid thermally-grown silicon dioxide post [Fig. 2(b)]. The advantages of only using two trenches are the higher aspect ratio of the resulting structure and the guarantee that the silicon ring between the two trenches is completely consumed during the oxidation step. Further, this allows to close the vertical gaps only by thermal oxidation. As soon as more than two trenches are used, this is practically impossible to achieve. For example, in the case of three trenches, either the gaps close before the silicon rings get completely consumed, which degrades the electrical insulation capability of the structure, or the trench between two silicon rings can not be closed by further oxidation.

The inevitable v-shaped grooves [Fig. 2(b)] are filled in an LPCVD tetraethoxysilane (TEOS) deposition step, to avoid dishing and erosion effects during the subsequent chemical-mechanical polishing (CMP) step [Fig. 2(c)].

Then standard lithography steps are used to pattern the oxide [Fig. 2(d)] and to reduce the height of the center post [Figs. 1(e)-(f)]. In another DRIE step [Fig. 2(e)] the structure is only partially released from the substrate. This is required because of the compressive nature of the thermally grown silicon dioxide. Fig. 3(a) shows an SEM photograph of an exemplary insulation structure. A profile measurement result [Fig. 3(b)] from a white light profiler (Model NewView 100, Zygo Corporation, Middlefield, CT) verifies the successful fabrication of a thermally-grown silicon dioxide structure, which is partially released and more than 30 μm deep extended into the conductive substrate.

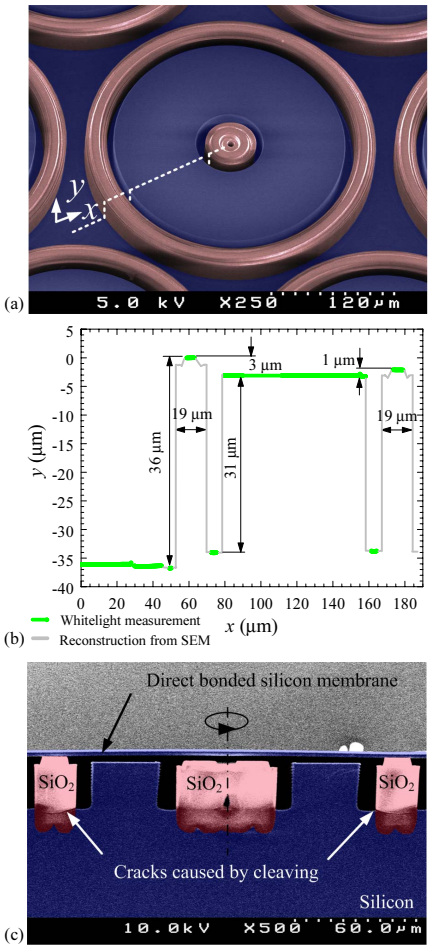

Fig. 3. Fabrication results: (a) Colorized SEM photograph (red…solid silicon dioxide, blue…heavily doped silicon) after the release step of one exemplary configuration fabricated. The dashed line outlines the location of the white light profiler measurement, shown in (b). (c) Colorized SEM photograph of an exemplary cross-section (cleaved sample) after direct wafer bonding to an SOI wafer. The handle wafer and box-layer have been removed.

At this stage of the wafer the decision to fabricate a CMUT or a sophisticated back plate for a CUT can be made: For the CMUT fabrication this insulation layer structure [Fig. 3(a)] can be bonded to another wafer using the direct wafer bonding technique. This fabrication run is not finished yet, but a preliminary result is shown in Fig. 3(c).

For the finished CUT back plate fabrication run, an 80-nm thick oxide-nitride passivation layer was deposited on the front side of the wafer. Then the back plates were released from the substrate using another DRIE step, because circular back plates with 11.85 mm in diameter were fabricated. The final step was to evaporate a titanium-platinum electrode at the bottom side of the back plates before they were assembled together with a

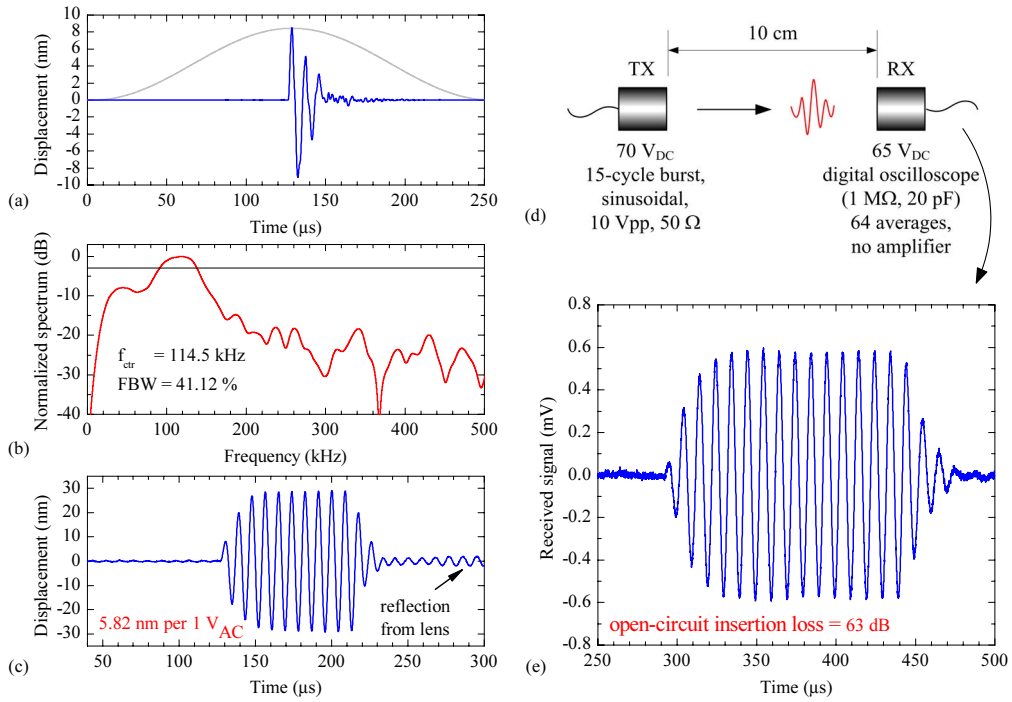

Fig. 4. Preliminary characterization results from a capacitive ultrasonic transducer featuring the back plate shown in Fig. 3(a). Impulse response (displacement) in time (a) and frequency domain (b) of a single cell. Response of a single cell to a 10-cycle sinusoidal burst signal at a center frequency of 114.5 kHz (c). Pitch-catch configuration (d) and measured received signal (e).

3 μm-thick metal membrane (TIMET 21S, Timet Ltd, UK) as top electrode material. First preliminary characterization results at room temperature are presented in Fig. 4.

IV. Conclusion

An extended insulation layer structure for CMUTs and CUTs was presented. It addresses electrical breakdown, parasitic charging, and parasitic capacitance issues. Besides significant improvements for the present CMUT and CUT technology, we expect that this extended insulation layer structure can improve many other electrostatic actuator/sensor devices in terms of reliability, performance, and high-temperature operation. For future work, we plan to test the fabricated CUTs at elevated temperatures and we aim to realize a high-temperature CMUT technology by finishing the CMUT fabrication run as outlined in this work.

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