Two-Dimensional Capacitive Micromachined Ultrasonic Transducer (CMUT) Arrays for a Miniature Integrated Volumetric Ultrasonic Imaging System

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ABSTRACT

We have designed, fabricated, and characterized two-dimensional 16x16-element capacitive micromachined ultrasonic transducer (CMUT) arrays. The CMUT array elements have a 250-μm pitch, and when tested in immersion, have a 5-MHz center frequency and 99% fractional bandwidth. The fabrication process is based on standard silicon micromachining techniques and therefore has the advantages of high yield, low cost, and ease of integration. The transducers have a Si_3N_4 membrane and are fabricated on a 400-μm thick silicon substrate. A low parasitic capacitance through-wafer via connects each CMUT element to a flip-chip bond pad on the back side of the wafer. Each through-wafer via is 20 μm in diameter and 400 μm deep. The interconnects form metal-insulator-semiconductor (MIS) junctions with the surrounding high-resistivity silicon substrate to establish isolation and to reduce parasitic capacitance. Each through-wafer via has less than 0.06 pF of parasitic capacitance. We have investigated a Au-In flip-chip bonding process to connect the 2D CMUT array to a custom integrated circuit (IC) with transmit and receive electronics. To develop this process, we fabricated fanout structures on silicon, and flip-chip bonded these test dies to a flat surface coated with gold. The average series resistance per bump is about 3 Ohms, and 100% yield is obtained for a total of 30 bumps.

Keywords: Capacitive micromachined ultrasonic transducer, CMUT, Two-dimensional array, Ultrasonic imaging, Through-wafer interconnect, Integration, Flip-chip bonding

1. INTRODUCTION

Since its invention in the mid 1990s, the capacitive micromachined ultrasonic transducer (CMUT) has become an increasingly promising alternative to the piezoelectric transducer. A CMUT is composed of a thin membrane supported by sidewalls over a thin cavity. Typically, many membranes are connected in parallel to form a single element. These membranes are coated with a layer of metal, and form capacitors with the back plate (Fig. 1). The membranes are biased with a DC voltage, and vibrate when an AC voltage is applied, thus generating ultrasonic waves. These capacitors are also used to sense impinging ultrasonic waves. If the electric field across the cavity of the CMUT reaches the magnitude of about 10^8 V/m, the CMUT becomes an efficient electromechanical transduction mechanism [1]. Modern micromechanical electrical systems (MEMS) technology enables the fabrication of vacuum cavities with heights of less than 0.1 μm. Electrical field strength on the order of 10^8 V/m is easily achieved by applying a few tens of DC bias volts across the vacuum cavity. In addition to the high transduction efficiency, CMUTs have wide bandwidth in immersion applications, and can be easily fabricated to cover a broad range of operating frequencies. Moreover, inherent to the standard silicon micromachining process, CMUTs enjoy high yield, high uniformity and low unit cost. Finally, CMUTs can be integrated with the front-end electronics using interconnection techniques such as through-wafer vias and flip-chip bonding. These integration methods can be compact, and with the inclusion of front-end electronics, mitigate the losses due to connecting cables.

This paper discusses the design, fabrication and characterization of a 2D 16x16-element CMUT array for a miniature real-time volumetric medical imaging system (Fig. 2) [2]. This system is intended for use in a 5-mm endoscopic channel. Section 2 describes the CMUT design and fabrication process. The characterization of the devices is presented in Section 3, followed by the system integration considerations in Section 4, and the conclusion in Section 5.

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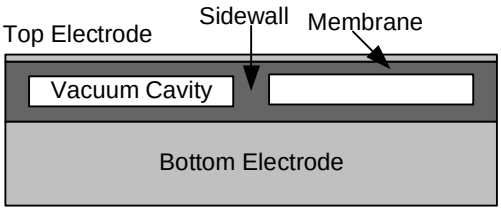


Figure 1: A simplified schematic of a CMUT.

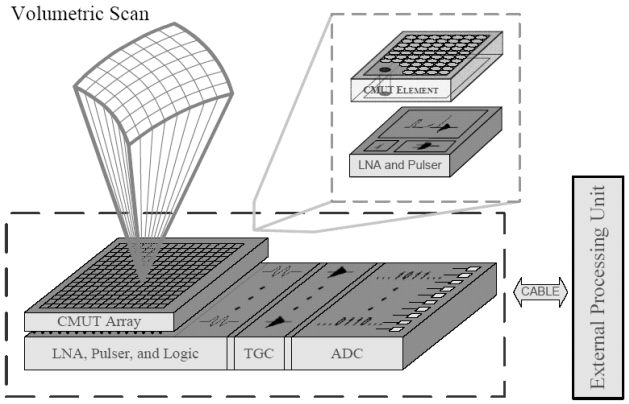


Figure 2: Miniature real-time volumetric imaging system based on 2D CMUT array.

2. DESIGN AND FABRICATION

2.1. CMUT Design

The transducer array is designed to have a center frequency of 5 MHz in immersion operation, and an element pitch of 150-μm or 250-μm. The 150-μm version is intended for use in a 5-mm endoscopic channel. Mason's electrical equivalent circuit model of a CMUT [3], shown in Fig. 3, helps guide the design of the CMUT. A detailed discussion of the equivalent circuit model can be found in [4]. On the electrical side of the equivalent circuit model, C_o is the CMUT capacitance and C_p is the parasitic capacitance. On the acoustical side, Z_{med} and Z_{memb} are the mechanical impedance of the surrounding medium and the membrane, respectively. The membrane size, thickness and material properties determine Z_{memb}, and thus the operating frequency of the CMUT. In immersion the medium impedance has a large resistive component. This large medium resistance overdamps the resonant circuit, and results in a wide bandwidth. The transformer represents the electro-acoustical conversion between the two ports. An analytical tool was developed based on this equivalent circuit model to facilitate the design process. Table I summarizes the key parameters for the designs in two fabrication cycles. Various membrane sizes were fabricated to cover a wide range of operating frequencies in a single fabrication run.

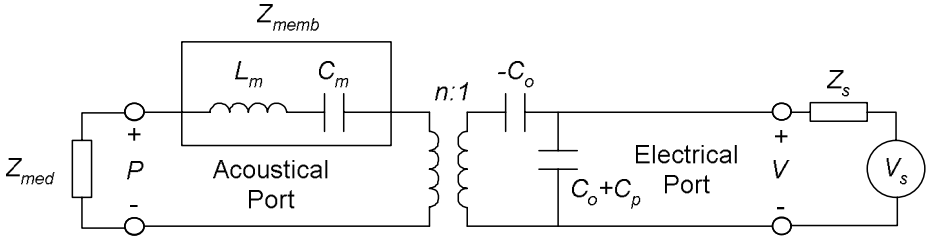


Figure 3: CMUT equivalent circuit in transmit.

Table I: Key process parameters.

Cell diameters, μm	24, 30, 36
Element pitch, μm	150, 250
Number of cells per element	24, 35, 48
Membrane thickness, μm	0.6, 0.8
Cavity thickness, μm	0.1
Insulating layer thickness, μm	0.15
Silicon substrate thickness, μm	400
Flip-chip bond pad diameter, μm	50
Through-wafer interconnect diameter, μm	20
Silicon wafer resistivity, Ω-cm	> 10,000

2.2. CMUT Fabrication

The sacrificial layer etch process [5] is used to fabricate these CMUTs. The metal-insulator-semiconductor (MIS) through-wafer interconnects [6] are used to connect each individual array element to the flip-chip bond pad on the back side of the wafer. In contrast to other through-wafer interconnect schemes [7, 8], the MIS through-wafer interconnects enable both DC bias polarities and high bias voltages. The latter feature is particularly desirable in this application, because in the final imaging system, a 30-V electrical pulse superimposed on a DC bias voltage is applied across the electrodes of the CMUTs. MIS through-wafer vias built on ultra-high-resistivity silicon wafers (ρ > 10,000 Ω-cm) resulted in a low via parasitic capacitance of 60 fF. This is approximately eight times lower than achieved previously [6]. The packing density of the through-wafer interconnects was also increased by about eight times [5-8].

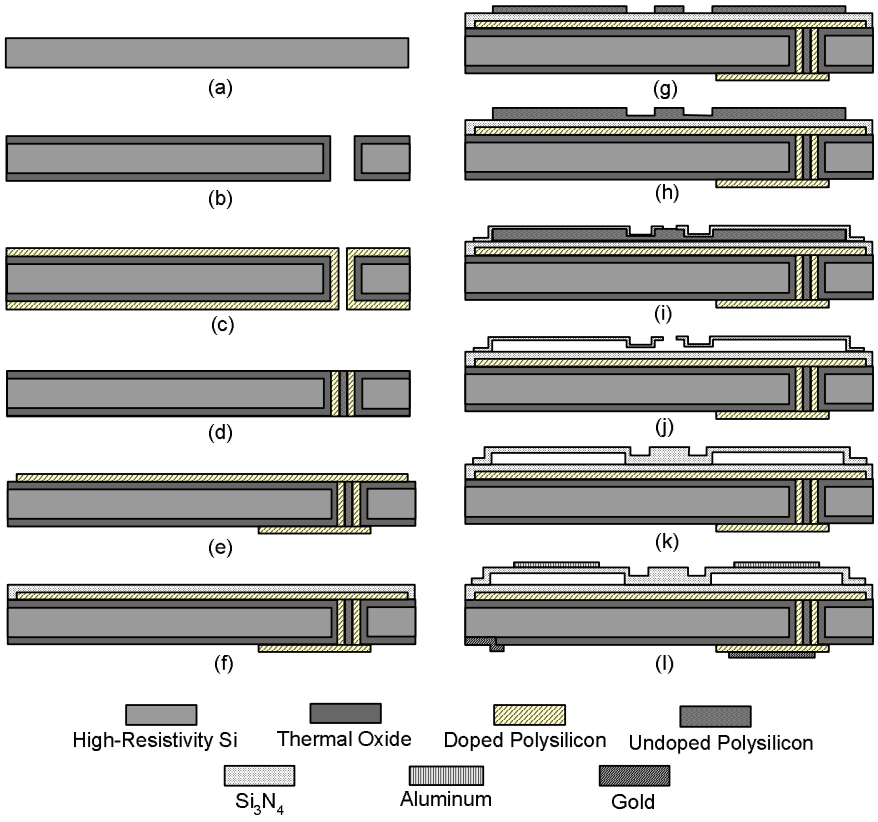


Figure 4: Process flow of CMUT fabrication.

The CMUT fabrication process starts with a double-side polished, 400-μm thick, p-type high-resistivity silicon wafer [Fig. 4(a)]. Deep reactive ion etching (DRIE) is used to etch 20-μm diameter through-wafer vias on the wafer. To achieve a better aspect ratio, the etching is performed from both sides of the wafer. A 1-μm thick thermal oxide layer is grown [Fig. 4(b)], followed by the low-pressure chemical vapor deposition (LPCVD) of a 2-μm thick polysilicon layer and phosphorous doping [Fig. 4(c)]. The purpose of the doping is to reduce the resistivity of the polysilicon. Undoped LPCVD polysilicon is grown on the wafer to fill the through-wafer vias, and the wafer is etched back to the oxide layer [Fig. 4(d)]. Another layer of 1-μm thick polysilicon is deposited, doped, and etched to form the active areas on the front side and the flip-chip bond pads on the back [Fig. 4(e)]. A layer of 0.15-μm thick Si_3N_4 film is grown on the front side [Fig. 4(f)] to provide etch stop for later steps when the polysilicon sacrificial layer is etched in the potassium hydroxide (KOH) solution.

A polysilicon sacrificial layer is deposited and patterned in two steps [Fig. 4(g), 4(h)] to define the cavities of the CMUTs and to reduce the height of the KOH etch channels. Reducing the height of the KOH etch channels improves the sealing quality of the cavities, and reduces undesired nitride deposition inside the cavities [5]. The typical cavity height is 0.1 μm to 0.15 μm; the KOH etch channel height is 0.05 μm. The cavities have diameters of 24 μm, 30 μm and 36 μm for different operating frequencies. Another Si_3N_4 film is grown on top of the sacrificial polysilicon layer. Using plasma etch, a 5-μm etch hole is defined on the Si_3N_4 film [Fig. 4(i)]. The polysilicon sacrificial layer is then etched away in KOH solution [Fig. 4(j)]. The etch hole is sealed with an additional 0.8-μm Si_3N_4 deposition [Fig. 4(k)]. The final membrane thickness of 0.6 μm to 0.8 μm is achieved by carefully etching back the Si_3N_4 film. After sputtering aluminum on the membrane to form the top electrode, and depositing gold on the polysilicon pads [Fig. 4(l)], the 2D CMUT arrays are diced and tested.

Fig. 5 shows different pictures of one 2D array: Fig. 5(a) is the front side view of the whole array; Fig. 5(b) is the magnified view of four array elements; Fig. 5(c) shows the details of the membrane and the through-wafer via; Fig. 5(d) illustrates the back side of four elements; Fig. 5(e) depicts the cross-section of the through-wafer vias.

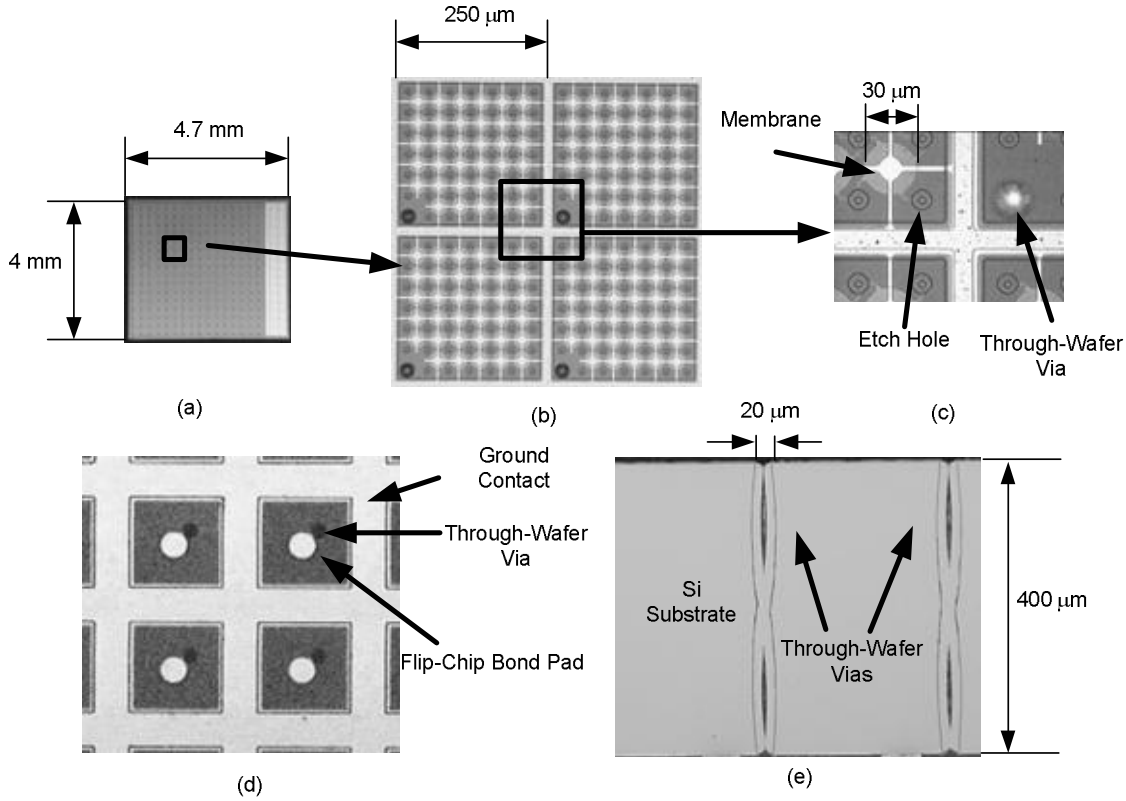


Figure 5: Pictures of a 2D array, array elements and through-wafer vias.

3. CHARACTERIZATION

Various test structures are included in the mask layout to independently characterize the CMUT elements and the through-wafer interconnects. To easily test the performance of the CMUTs, array elements without the through-wafer interconnects are fabricated on the same wafer as the regular 2D arrays. Stand-alone through-wafer interconnects are also fabricated on the same wafer to test the interconnect resistance and capacitance.

3.1. Characterization of CMUTs

The 2D CMUT arrays were characterized in air as well as in immersion. A network analyzer (Model 8751, Hewlett-Packard Company, Palo Alto, CA) was used to measure the input impedance of the array elements in air. Capacitance values were then extracted from the impedance measurements. The sum of the device capacitance and the interconnect parasitic capacitance is 1.3 pF for an array element composed of 30-μm diameter membranes. This measurement was carried out under a 20-V DC bias. The total capacitance is reduced to 1.0 pF under a negative 20-V DC bias. The difference of 0.3 pF is due to the change in the parasitic capacitance of the through-wafer interconnect under different bias polarities (Section 3.2). To test for uniformity, an element-by-element impedance measurement was carried out on a typical 2D array in air. Fig. 6 shows the resonant frequency distribution of the 256 elements, and Fig. 7 is the capacitance distribution. The average resonant frequency is 13.4 MHz with a standard deviation of 0.5%. The average capacitance for a single element is 1.3 pF with a standard deviation of 7%. Deducting the parasitic capacitance of the through-wafer interconnect from the total capacitance, the CMUT capacitance is calculated to be 0.8 pF.

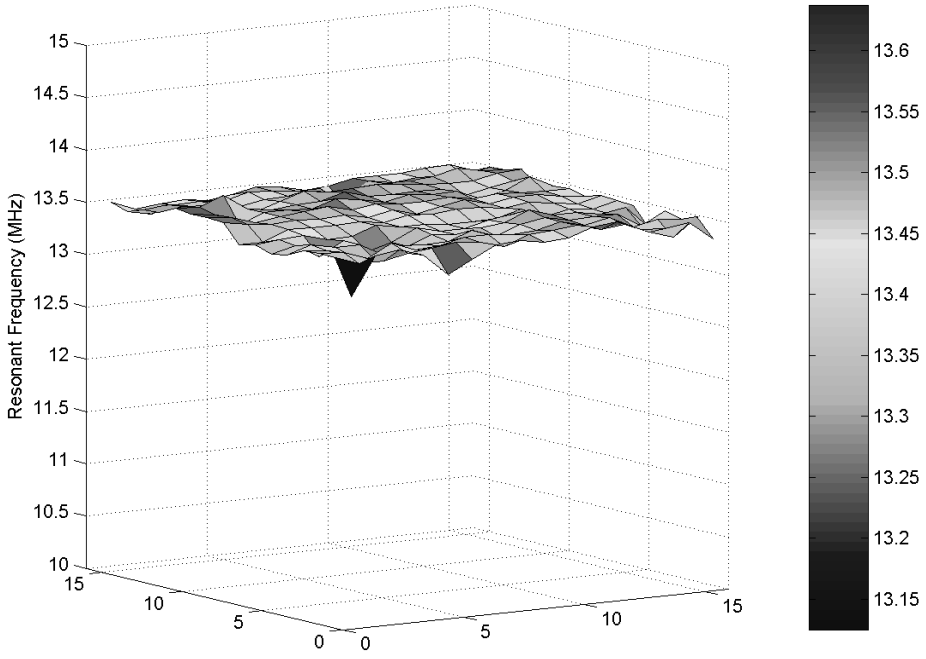


Figure 6: Resonant frequency distribution across a 2D CMUT array.

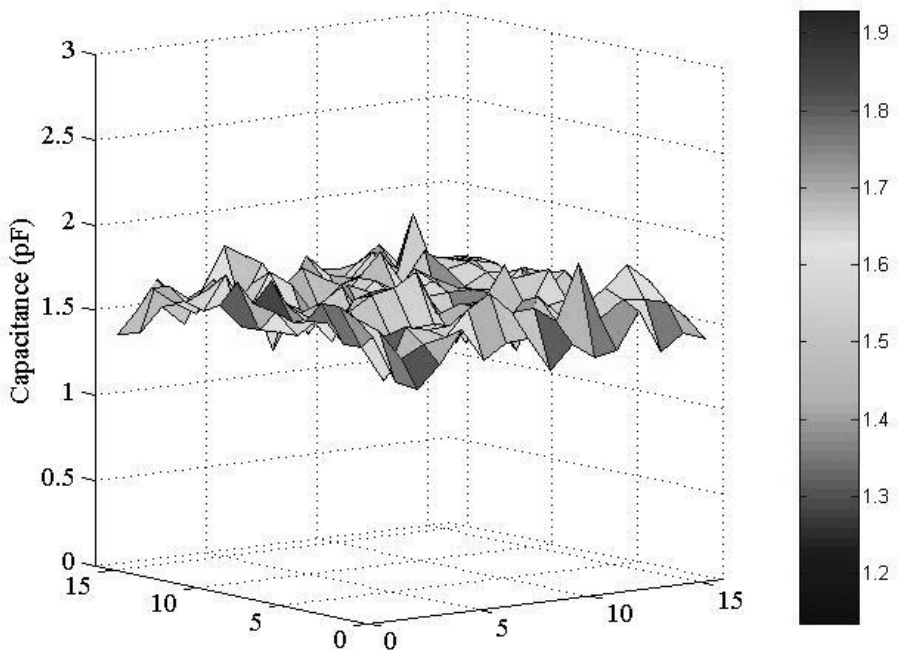


Figure 7: Total capacitance distribution across a 2D CMUT array.

The devices were also tested in immersion. In the pitch-catch measurements, the device was placed 10 mm away from a calibrated hydrophone (Model PZT-Z44-0400, Specialty Engineering Associates, Sunnyvale, CA). The hydrophone was positioned by a linear stage (Model HDZ2, Aerotech Inc., Pittsburgh, PA) with an accuracy of 1 µm. A 17-dB, 10-kHz to 25-MHz, 50-Ω preamplifier amplified the hydrophone signal before it was read into a digital oscilloscope (Model 54825A, Hewlett-Packard Company, Palo Alto, CA). The device was biased at 30-V DC. A 30-V unipolar pulse with a pulse width of 100 ns was applied to the device, and the oscilloscope readings were recorded [Fig. 8(a)]. The Fourier transform of the hydrophone response, after correcting for the medium attenuation, diffraction, and hydrophone response, has a center frequency close to the design target of 5 MHz, and a 3-dB fractional bandwidth of 99% [Fig. 8(b)]. The peak output pressure, extrapolated to the surface of the transducers, was 100 kPa when excited with a 100-ns, 30-V pulse.

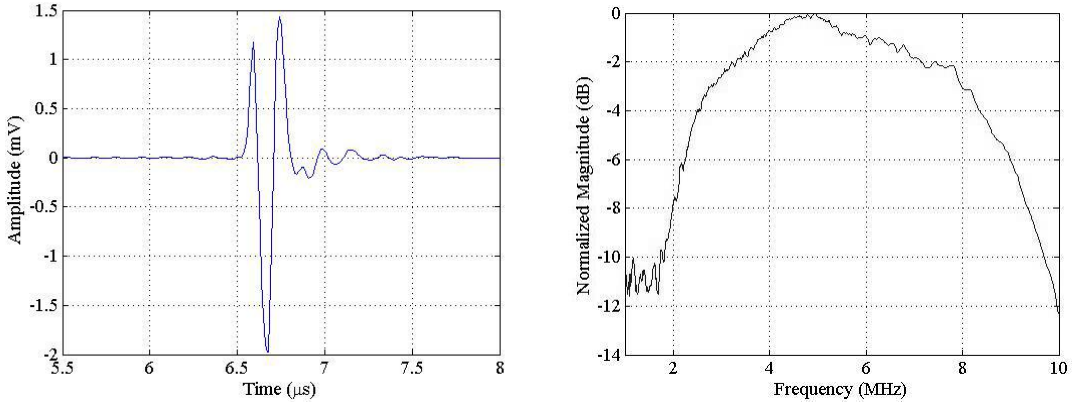
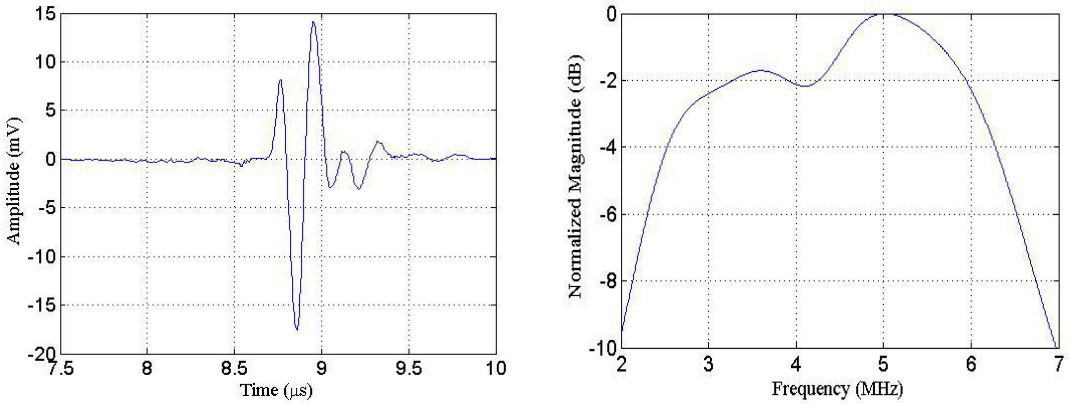


Figure 8: (a) Response of the CMUT to a pulse excitation in vegetable oil, (b) Fourier transform of the response, corrected for medium attenuation, diffraction, and hydrophone response.

Finally, an array element was wire bonded to a custom transmit and receive IC die. The device was then immersed in vegetable oil, resulting in an oil/air interface 6.6 mm in front of the transducer surface. The CMUT was biased at 30-V DC, and excited by the IC with a 100-ns, 30-V unipolar pulse. After the excitation, the IC switched into the receiving mode to detect the ultrasonic wave reflected back from the oil/air interface. Fig. 9 shows the pulse-echo signal and the uncorrected Fourier transform. The 6-dB fractional bandwidth is 97%. A 2D CMUT array will be flip-chip bonded in the near future to the same IC, and a volumetric image will be demonstrated.



(a) (b)

Figure 9: (a) Pulse-echo measurement of the CMUT with custom IC, (b) uncorrected Fourier transform.

3.2. Characterization of Through-Wafer Interconnects

The metal-insulator-semiconductor structure is extensively studied in semiconductor solid-state physics [9]. The high-frequency capacitance of such a structure depends on whether it is operated in the accumulation region or inversion region, and can be expressed as

$$C_{accumulation} = C_O = \frac{K_O \varepsilon_o A}{x_o}, \qquad (1)$$

$$C_{inversion} = \frac{C_O}{1 + \frac{K_O W_T}{K_S x_o}}, \qquad (2)$$

where C_O is the parallel plate capacitance of the insulator, K_O is the insulator dielectric constant, ε_o is the permittivity of the free space, A is the electrode area, x_o is the insulator thickness, W_T is the maximum depletion width in the bulk silicon, and K_S is the silicon dielectric constant. It is shown in [9] that

$$W_T \propto \sqrt{1/N_A}\,. \qquad (3)$$

There are two methods to reduce the parasitic capacitance associated with the MIS interconnect: the first is to reduce the electrode area A; the second is to increase the maximum depletion depth W_T, by using a high-resistivity wafer. To reduce the electrode area, the polysilicon flip-chip bond pads at the back side of the wafer are designed in such a way that the total area is as small as possible. The design requires a 5-μm safety margin to accommodate any alignment uncertainties. Fig. 10 shows a picture of the flip-chip bond pad. To achieve a large W_T, ultra-high-resistivity wafers (ρ > 10,000 Ω-cm) are used.

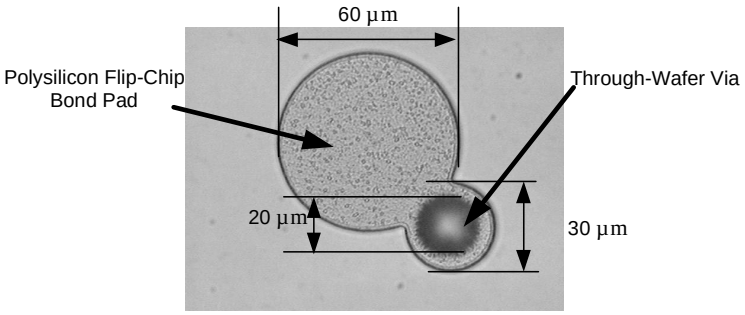


Figure 10: Picture of a polysilicon pad with minimal area.

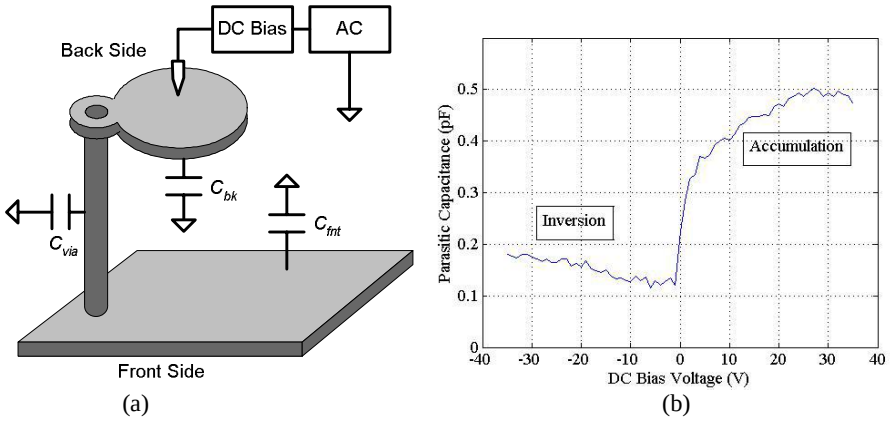


Figure 11: (a) Schematic of the parasitic capacitance measurement setup, (b) parasitic capacitance as a function of DC voltage.

Fig. 11(a) shows the schematic of the parasitic capacitance measurement setup. The total interconnect parasitic capacitance is composed of the front side pad capacitance (C_{fnt}), the via capacitance (C_{via}), and the back side pad capacitance (C_{bk}). Under positive DC bias, the p-type silicon substrate is in accumulation, and the total interconnect parasitic capacitance is 0.5 pF; under negative DC bias, the silicon substrate enters inversion, and the capacitance is reduced to less than 0.2 pF. Based on the MIS junction area percentage, the via capacitance is calculated to be less than 60 fF. Normalized to the area, the parasitic capacitance of the MIS through-wafer interconnect has been reduced by 7.4 times from the previously reported values [6]. Each through-wafer interconnect has a resistance of 20 Ω. Fig. 12 shows the test structure and the setup for measuring this resistance. At a 5-MHz operating frequency, the CMUT presents a high impedance, and the interconnect resistance can be safely ignored.

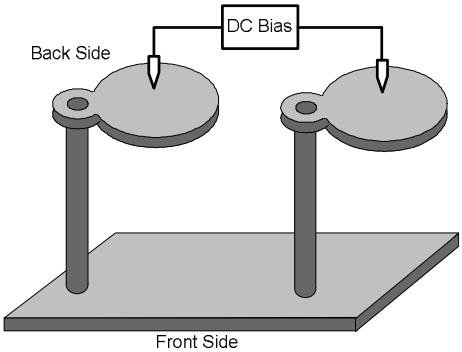


Figure 12: Schematic of series resistance measurement setup.

4. SYSTEM INTEGRATION CONSIDERATIONS

Through-wafer interconnects and flip-chip bonding compactly connect large two-dimensional arrays with the front-end electronics. This integration can lead to significant improvement in signal-to-noise ratio by reducing the lengths of connecting cables between the transducer elements and preamplifiers. A Au-In flip-chip bonding process [Fig. 13(a)] was investigated for this purpose. The lift-off process was used to define the 0.3-µm thick Au layer on the back side pads of the CMUT array, and the Ti/Cu/Au/In layers on the aluminum pads of the IC dies. To test the yield and the bond resistance of this process, we fabricated fanout structures with the Ti/Cu/Au/In pads on silicon, and flip-chip bonded these test dies to a flat surface coated with Au. The bonding process was carried out in a manual bonder (Model M8, Research Devices Inc., Piscataway, NJ). The maximum pressure applied to the dies was 30 grams/bump, and the maximum temperature was 150 °C. After bonding, the attached dies underwent a thermal reflow at 200 °C on a hot plate for 5 minutes. Low viscosity epoxy (Type BA202, Tra-con Inc., Bedford, MA) was then applied as underfill between the two dies. The measured series resistance per bump was 1 Ω to 8 Ω, and 100% yield was obtained for a total of 30 bumps [Fig. 13(b)]. This method can be used to flip-chip bond the 2D CMUT arrays to the IC dies.

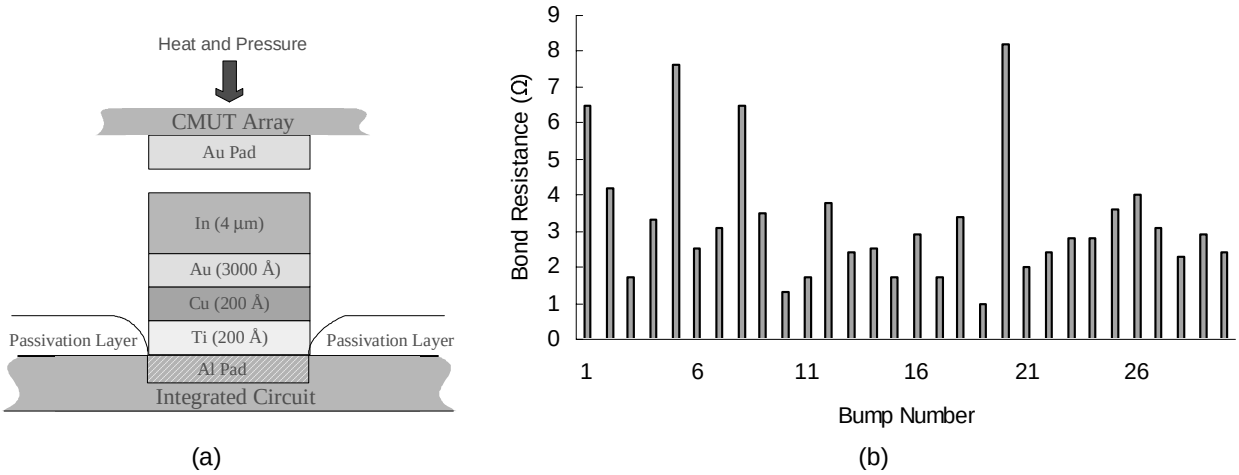


Figure 13: (a) Metal stack used for flip-chip bonding, (b) bond resistance.

5. CONCLUSION

Two-dimensional 16x16-element CMUT arrays with through-wafer interconnects were designed, fabricated, and tested. The arrays with 150-µm element pitch are suitable for a miniature volumetric medical imaging system used in a 5-mm endoscopic channel. The fabricated devices present uniform resonant frequencies when measured in air. When tested in immersion, the center frequency is close to 5 MHz, and the 3-dB fractional bandwidth is 99%. The peak output pressure at the surface of the transducer is 100 kPa when excited by a 100-ns, 30-V pulse. Pulse-echo measurements were taken for the CMUT with a custom transmit and receive IC. The transducer elements are addressed individually by the through-wafer vias. The through-wafer via has a parasitic capacitance of less than 60 fF, and a series resistance of 20 Ω. Preliminary tests show a Au-In flip-chip bonding process provides low bond resistance and 100% yield. A real-time volumetric imaging system based on these 2D CMUT arrays will be demonstrated in the near future.

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