Fabrication and Characterization of 1-Dimensional and 2-Dimensional Capacitive Micromachined Ultrasonic Transducer (CMUT) Arrays for 2-Dimensional and Volumetric Ultrasonic Imaging

A. S. Ergun, C-H. Cheng, U. Demirci, and B. T. Khuri-Yakub
E. L. Ginzton Laboratory, Stanford University
Stanford, CA, 94305-4088
sanli@stanford.edu

Abstract-**Capacitive Micromachined Ultrasonic Transducers (CMUTs) were introduced about a decade ago as an alternate method of generating and detecting ultrasound. Since their introduction, considerable research has been done to characterize CMUTs. They have been shown to have broad frequency bandwidth and very good sensitivity. Besides, CMUTs are built on silicon using standard surface micromachining techniques, and therefore have all the advantages of IC processing, such as parallel production, batch fabrication and very high level of integration. All these qualities made CMUTs and CMUT arrays an alternative to their piezoelectric counterparts. In this paper, we focus on the CMUT fabrication process and present recent advances which made it possible to achieve very high process yields (practically 100%) leading to the fabrication of fully functional one-dimensional (1D) and two-dimensional (2D) CMUT arrays. Because of limitations on the element size, the fabrication of 2D CMUT arrays involves the use of electrical through-wafer interconnects (ETWI) which brings the electrical connection of each element from the transducer side to the backside of the wafer. In this paper, we also present ETWIs that have parasitic capacitance as low as 0.25 pF integrated with a 2D CMUT array of 128 by 128 elements. These arrays are characterized and tested in real imaging cases. The paper concludes with the presentation of the sample imaging results that demonstrate the viability of the CMUT process for array fabrication.**

I. INTRODUCTION

Since its first introduction [1-4] CMUTs have been considered as an alternative to piezoelectric transducers in many areas of application, because of the advantages they provide. Some of these advantages can be attributed to the simple fact that CMUTs are made of a plurality of thin membranes that are fully supported on all sides with insulating posts [1-7]. The mechanical impedance of such thin membranes is much smaller than those of fluids in a wide frequency range. This fact makes otherwise resonant CMUTs wideband transducers in immersion applications, which is one of the major advantages over piezoelectric transducers. Research in this matter has shown that CMUTs indeed have wide frequency bandwidth characteristics [3,7, 9-11].

One other important feature of the CMUTs is the fabrication process that is used to build them. Micromachining has emerged through the silicon integrated circuit (IC) technology. It uses the same standard tools, such as photolithography, thin film deposition and plasma etching. Therefore, it has all the advantages that the IC processing technology provides, such as parallel processing, batch fabrication and very high level of integration. The implication of this fact is that it takes the same amount of effort to build a single element device and a 128 element array. However, another issue emerges when one starts to fabricate arrays, which is the functional yield of the array.

Although 64 and 128 element CMUT arrays have been fabricated and characterized [9,10], imaging experiments were done only with a 16 element sub-array [11] because of the yield issues. This paper discusses the problems with the yield of the CMUT arrays, and their solutions. We will describe the revised fabrication process that improves the yield to practically 100 %. We will start with briefly reminding the principle of operation of the CMUTs. Then, we will go into the details of the new fabrication process. Building 2D CMUT arrays is more complicated than 1D arrays because of the electrical interconnection difficulties to individual array elements. In Section V, we will describe how we integrate the CMUT process with the ETWI process to solve the electrical addressing problem of 2D transducer arrays [12]. We will show some results demonstrating the yield of the process, and finally draw some conclusions.

II. PRINCIPLE OF OPERATION

CMUTs are made of silicon nitride (Si_3N_4) membranes that are supported on all sides above a conductive silicon substrate. The gap between the membrane and the silicon substrate is vacuum sealed for immersion applications. Another electrode is deposited on top of the Si_3N_4 membrane which creates a parallel plate capacitor with the conductive silicon substrate as shown in Fig. 1.

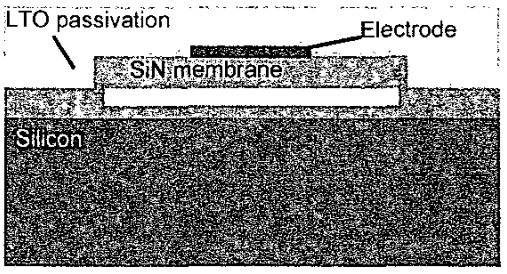


Fig. 1: A schematic cross-section of a membrane.

This work is sponsored by Office of Naval Research.

The principle of operation of CMUTs in transmit relies on the electrostatic attraction force between charges of opposite polarities. When a DC voltage is applied to the electrodes of the membrane, the membrane deflects towards the substrate which is the ground electrode. The electrostatic attraction force is balanced by the restoring force of the mechanical spring formed by the membrane. Then, one can imagine vibrating the membrane by adding a small AC signal on top of the DC signal. A vibrating membrane then couples mechanical energy into the surrounding medium. On receive the membrane vibrations are converted into electrical current by applying a DC voltage across the CMUT. The capacitance variation of the CMUT caused by the membrane vibrations generates a current in the external circuit. This current is converted into voltage across a resistor and then amplified for further processing. The details of CMUT operation can be found in many publications [1-3].

The measure of the efficiency of the CMUT is the electromechanical coupling efficiency which shows how efficient the electrical energy is converted into mechanical energy. It turns out that, as shown in [17], the electromechanical coupling efficiency increases with increasing electrical field inside the gap (or equivalently DC bias voltage) and becomes 100 % at the collapse voltage of the membranes. The collapse of the membranes occurs when the restoring force of the mechanical spring cannot balance the electrostatic attraction force. The voltage creating this much electric field is called the collapse voltage. Unable to vibrate after collapsing the membranes neither transmit nor receive ultrasound. Therefore, CMUTs are always operated below the collapse voltage but very close to it to ensure efficient operation.

III. Fabrication Process

The main principle of building membranes that are supported on all sides above a substrate is first depositing or growing a sacrificial layer on the substrate. Then, this sacrificial layer is covered with the membrane material, and removed with wet etch through holes in the membrane. This principle stayed the same throughout the evolution of the conventional CMUT fabrication, but the way of defining the sacrificial layer changed.

A. Active Area Definition

The active area of a CMUT is defined as the moving area, which is the same as the cavity beneath the membrane. When CMUTs were first introduced, the sacrificial layer was made of a blank thermally grown silicon dioxide (SiO_2) layer. The sacrificial SiO_2 layer was covered with the Si_3N_4 membrane, and then removed with wet etch. The size of the cavity and the membrane was determined by a timed etch [1][2]. Later, this process was changed. Researchers started patterning the sacrificial layer prior to the membrane deposition [3][5][6], so that the size of the membrane was determined by a photolithography followed by a Reactive Ion Etch (RIE) step rather than a timed etch which is rather critical. Research on the choice of the membrane and the sacrificial layer [7]

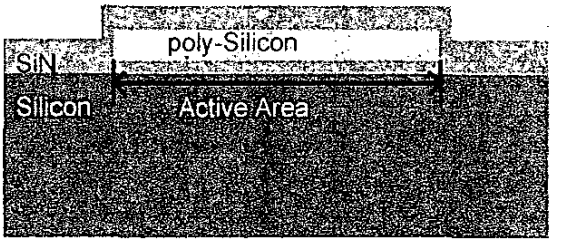


Fig. 2: Cross-section of a membrane after sacrificial poly-silicon layer deposition and patterning. Then, the sacrificial layer is coated with LPCVD Si3N4 which conformably covers the edges as well.

revealed that the best choice is Low Pressure Chemical Vapor Deposited (LPCVD) Si_3N_4 and LPCVD poly-silicon respectively, as shown in Fig. 2. As it is clear from the figure, there is another layer of Si_3N_4 under the sacrificial poly-Silicon layer. This thin Si_3N_4 layer is an etch stop for the wet etch of the sacrificial layer which will be discussed later.

The membrane size and its thickness are the parameters that determine the static and dynamic characteristic of the transducer. They are designed and fabricated according to the frequency of operation, DC operating voltage, and ambient pressure conditions.

B. Cavity (Gap) Definition

The cavity between the membrane and the substrate is defined at the same time as the active area. The lateral dimensions of the cavity are equivalent to that of the sacrificial layer. The thickness of the gap is determined by the thickness of the sacrificial poly-silicon layer that is grown by LPCVD. The cavity depth has important implications on the process flow, especially in the wet release of the membrane. These implications will be discussed later.

The cavity depth primarily determines the operating voltage and maximum tolerable ambient pressure. It also determines the maximum membrane vibration amplitude and so the maximum output pressure rating. The cavity depth is designed according to these criteria. In general, immersion transducers are designed with smaller gap because the range of motion for the membrane is rather small, whereas in air the vibration amplitude can be very large. Typically, the cavity depth for immersion transducers is 1000 Å.

C. Sacrificial Layer Etch

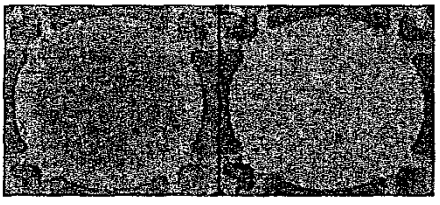
After the membrane deposition as described in subsection *A*, the sacrificial poly-silicon layer becomes sandwiched between Si_3N_4 layers. To be able to remove the poly-silicon layer, one has to open a hole through the Si_3N_4 to get access to the sacrificial layer, which is called the etch via. Then, the whole wafer is immersed in a wet etchant which selectively etches the sacrificial layer, and does not etch the Si_3N_4 membrane. In the case of poly-silicon sacrificial layer, this etchant is potassium hydroxide (KOH) which has a very good selectivity between poly-silicon and Si_3N_4 (~400000:1). This step is the most time consuming step which can take up to several days, and the most critical one as well. There are two kinds of difficulties at this step. One of them is releasing of the stress inherent in the sacrificial layer and the membrane.

This effect is most critical for large membrane sizes, typically for membranes larger than 100 μm in diameter, and ends up breaking the membranes. Immersion transducers for imaging applications in the MHz range usually consist of membranes that are much smaller in diameter, and therefore do not suffer from this problem.

The other difficulty is the drying of the fluid inside the cavity after the wet etch process. Following the removal of all the sacrificial poly-silicon, the wet etchant is removed and replaced with deionized (DI) water. Then, the DI water has to be dried. During the evaporation of the DI water the capillary forces pull the membrane towards the substrate. If the mechanical spring constant of the membrane is not stiff enough, these forces may stick the membrane to the substrate which is mostly irreversible [13-15]. The capillary force affecting each membrane is proportional to the area and inversely proportional to the cavity depth. That is, large membranes with small gaps are more likely to have this problem. Fig. 3 demonstrates this problem, where (a) shows a collapsed membrane after the wet release process, and (b) shows a membrane that released safely. As an example, in this particular case the membrane diameter is 36 μm, and the cavity depth is 1250 Å. The collapsed membrane has a thickness of 0.1 μm where as the other one is 0.4 μm thick.

D. Etch Channel Definition

After the removal of the sacrificial layer the sealing of the membranes is done via another thin film deposition. The deposition is done until the etch hole is completely plugged. Since this deposition step is done under vacuum, the cavity is vacuum sealed in the end. Two kinds of material became practical for this purpose, which are LPCVD grown Si_3N_4, and Low-Temperature Oxide (LTO) [6]. It is found that LPCVD Si_3N_4 has a very low sticking coefficient, which means it can easily go through small holes and channels. It eventually seals the etch hole, but deposits inside the cavity too. On the other hand, LPCVD LTO has a higher sticking coefficient which means it does not like to go in through holes, and cavities. It does not deposit anything inside the cavity, but it may take a very long time to seal depending on the channel and hole dimensions. In some cases, it may not seal at all. For this reason Si_3N_4 is preferred against LTO for sealing, but several precautions are taken against the Si3N4 deposition inside the cavity.



(a) (b)

Fig. 3: Two membrane pictures after the wet release process, (a) 0.1 μm thick membrane collapsed after the wet release, (b) 0.4 μm thick membrane released safely.

In the first versions of the CMUT fabrication process, the etch via was located on the membrane [1-3,5,6]. That is, after the release process the membrane ended up with holes through it. Sealing of such membranes was rather difficult because of the material deposition inside the gap. Later, researchers started to use labyrinth-like etch channels to make the path length to the cavity long and complicated [7] as seen in Fig. 4. The larger circles on four corners are the membranes, and the structure in the middle is the etch channel that serves these four membranes. The etch hole is located in the middle of the etch channel structure. In this way, it was possible to seal the etch channels without depositing much Si_3N_4 inside the cavity. These etch channels are defined at the same time with the active area, and they are made of poly-silicon too. The wet etch starts through the etch hole, and proceeds through the channels.

One down side of this is the increase in the wet release time because of the increase in the path length that leads to the cavity. Another down side is that after the sealing process the membranes keep connected through the channels. The reason is that sealing process takes place very close to the etch hole, and leaves the channels open. This is an important problem in terms of the functional yield. In 1D array elements there are typically 1000 membranes per element. With this kind of etch channel structure, if the vacuum seal of one membrane fails, then all of the 1000 membranes fail. In other words, one defect on a membrane or in a channel, which are typical problems, is amplified by the total number of membranes in an element. The functional yield of the whole array drops by a factor of 1000 from the overall yield of the membranes.

Even though the channels are designed to make it hard for the Si_3N_4 molecules to get into the cavity, there is still some Si_3N_4 deposition inside the cavity. In some cases this amount may be tolerable, but in array fabrication, where uniformity across the array elements and control over the membrane parameters is very critical this may not be enough. A further improvement to the sealing process is to decouple the cavity depth and the etch channel height. Normally, the etch channels and the active area are defined with a single lithography step. Therefore, the cavity depth and the etch channel height are equal. One can improve the sealing quality by reducing the etch channel height. To do this, the cavity

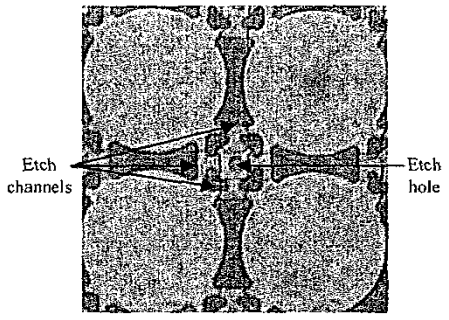


Fig. 4: An etch channel structure that is used to wet etch the sacrificial layer beneath the membranes.

depth and the channel height must be defined separately. This means an additional photolithography step, but improves the sealing quality considerably. Fig. 4 already shows the effect of this additional step. The green regions of the etch channel structure are the areas where the etch channel height is reduced. This is done right after the active area definition. Fig. 5 shows a schematic cross section of a membrane with the reduced channels. When done in this way, the etch channels seal much faster, and the Si_3N_4 deposition inside the cavity is minimal.

While sealing the etch channels with Si_3N_4 deposition, the same amount of Si_3N_4 gets deposited on top of the membrane. This may increase the membrane thickness considerably depending on the channel height. Later, the membrane is etched back to the desired thickness. The fast sealing of the channels actually means sealing with less Si_3N_4 deposition on the membrane. Therefore, it has implications on the following steps too. When the initial membrane thickness and the channel height are designed correctly, the membrane etch back step may even be avoided.

Although, reducing the channel height helps the sealing process, it does not solve the yield problem alone. The ultimate solution to the yield problem is to isolate the membranes from each other or to make sure that they become isolated after the sealing. Fig. 6 shows such an etch channel structure. The channels are long and have 90° bends to make the sealing process easier as described before, and their height is reduced for better sealing. The sealing takes place first at the edge of the reduced channel region as shown in Fig. 7, and the membranes all become isolated from each other. In this case, even if several membranes fail, the failure does not get amplified as in the previous case. The loss of a membrane causes slight loss in the overall device performance. However, this loss is very minimal both for 1D and 2D array elements.

E. Membrane Thickness Definition

The membrane thickness is one of the important parameters that affect the device performance as described earlier. It is determined by the initial membrane deposition, the sealing deposition and the membrane etch back step. Normally, due to the deposition steps, the membrane gets very thick, and has to be etched back. This is one of the steps

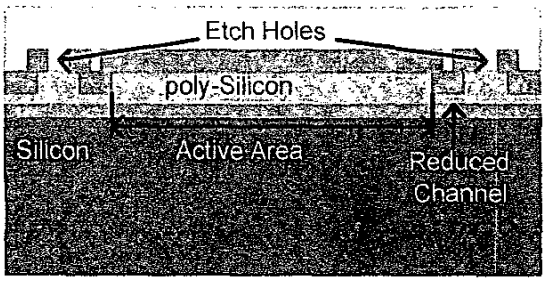


Fig. 5: Schematic cross section of a membrane after active area definition with the reduced channel height, and the membrane deposition. The etch holes are also shown.

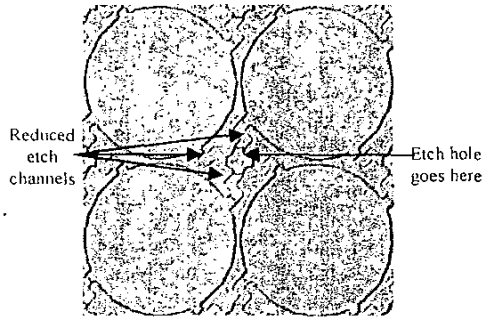


Fig. 6: A revised etch channel structure that is used to wet etch the sacrificial layer beneath the membranes.

where the functional yield gets a hit. Membrane etch back is done with RIE. When long etch backs are done, the nonuniformity of the RIE starts to affect the uniformity of the arrays. Therefore, reducing the channel height independent of the cavity depth and isolating the membranes increases the functional yield of the array in two ways.

F. Electrode Definition and Passivation

After the membranes reach their final thickness, another hole through the Si_3N_4 layer is opened to get access to the ground layer. Then, the wafer is coated with Aluminum (Al) and patterned to make up the top electrode. The top electrode is usually smaller than the active area. The reason for this is that the edges of the membranes do not move a lot, and any capacitance that is not moving is considered as parasitic capacitance. Minimizing the parasitic capacitance is crucial for the device performance [10], therefore one has to optimize the electrode size considering both the efficiency and the collapse voltage [16]. The final steps of the process are passivating the top electrode with LPCVD grown LTO, and patterning it to open bonding pads. The final cross-section of a membrane is shown in Fig. 1.

IV. One-Dimensional CMUT Arrays

The changes on the CMUT fabrication process was first experimented on 1D array process. The following are the design considerations for the 1D array.

A. Array Element Size

We fabricated 64 and 128 element 1D arrays. The width of each element is determined by the frequency of operation.

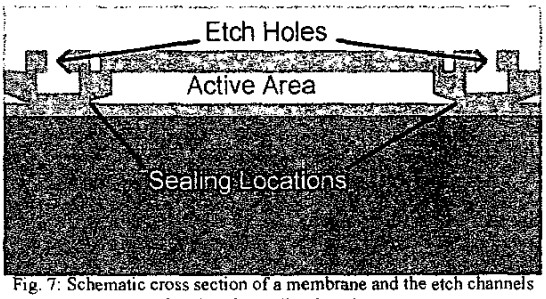


Fig. 7: Schematic cross section of a membrane and the etch channels showing the sealing locations.

These arrays were designed to operate around 3 MHz in immersion. Therefore element to element spacing is 250 μm which is equal to half wavelength at 3 MHz. The length of a 1D array element is chosen to be 6 mm to increase the signal transmitting and receiving capabilities.

B. Membrane Size

Membrane size is determined by simulations to give the best dynamic range, bandwidth, and lowest collapse voltage for low voltage operation. 36 μm diameter circular membranes were chosen as the basic building block of the array elements. Then, the total number of membranes in an array element becomes 800.

C. Cavity Depth and Membrane Thickness

The cavity depth was designed to be 1200 Å. To be able to release the membranes safely, the initial membrane thickness was chosen to be 0.6 μm. Including the Si_3N_4 thickness deposited for sealing, the total membrane thickness comes to 0.88 μm.

As a result of these improvements we were able to increase the functional yield of the CMUT process to 100 %. Fig. 8 shows a portion of a 1D array element. In this picture there are 4 array elements, each consisting of 800 membranes. Fig. 9 shows the resonance frequency of the array elements that are measured in air. Evidently, all the elements work. The fluctuations in the measurements are due to finite sampling in the frequency spectrum. However, there is evidently a slight decrease as the element number increases which is a reflection of the nonuniformity of the membrane thickness.

Although Fig. 9 shows that all the elements in the 128 element array works in air uniformly, it does not guarantee operation in immersion. To test the yield of the array in immersion, it is not possible to measure the resonance frequency because the resonance is over-damped. Instead, one of the elements (#1) fires an ultrasonic pulse, and all the rest listens to the echoes from a wire target in an immersion tank. Fig. 10 is an image of all the data received. The x-axis is the time axis which shows the arrival time of the echo signal, and y-axis is the element number. The color code represents the signal amplitude. This plot demonstrates that all of the 128 elements of the CMUT array work in immersion.

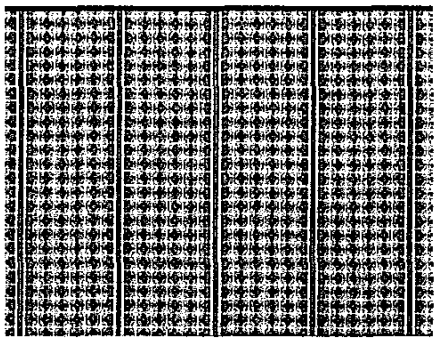


Fig. 8: A picture of a portion of a 1D CMUT array.

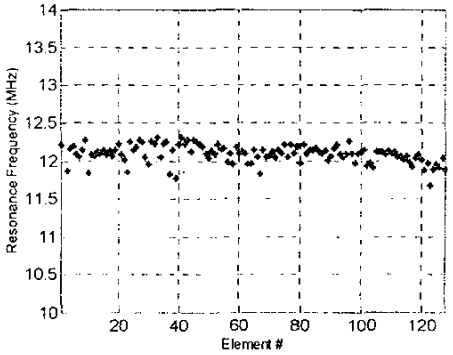


Fig. 9: Resonance frequencies measured from a 128 element 1D array.

V. Two-Dimensional CMUT Arrays

The fabrication of 2D CMUT arrays is a much more demanding task. The main problem associated with 2D arrays is the electrical addressing of individual array elements. When the element count is very small, electrical routing on the array surface may be an option at the expense of active area. However, for large element count arrays, surface routing is not even possible. Electrical through wafer interconnects finds an elegant solution to this problem by bringing the electrical connection of each array element to the backside of the silicon wafer. Then, the silicon wafer is flip chip bonded directly on to a front-end electronic IC. In this way, two things are accomplished at the same time. First of all an efficient interconnection scheme is realized and next the front-end electronics is brought to close proximity of the transducer array. The latter is of great importance, especially when the array elements are small. The device capacitance of a 2D array element is usually very small, 1 pF for the current application. Long interconnects and cables are all intolerable for this tiny capacitance.

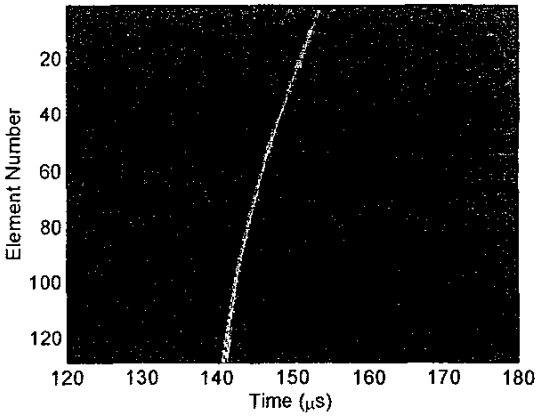


Fig. 10: The response of the array elements to single element (# 1) firing. The signal is reflected from a wire target in an immersion tank.

2D CMUT array fabrication starts with the fabrication of the ETWIs on a silicon wafer. The details of the ETWI process are described in [12]. Then, the usual CMUT process is done on this new silicon wafer with through wafer interconnects. Fig. 11 shows a schematic view of 2D array element with the dimensions. The challenge in this task is to make interconnects with the least parasitic capacitance. The through wafer via that is filled with doped poly-silicon, the front and backside pads all present a capacitance to the silicon substrate which is the ground. It was found that creating reverse-biased pn junctions underneath the pads and inside the through-wafer via gives the minimum possible parasitic capacitance. Practically, when a reverse bias is applied all the silicon substrate becomes depleted of free charges, and the parasitic capacitance reduces to merely a fringing capacitance between the signal and ground pads. By doing this we were able to achieve a parasitic capacitance as low as 0.05 pF for a through wafer interconnect, which is negligible compared to a CMUT array element (~1 pF).

128 by 128 element 2D CMUT arrays have been fabricated for underwater volumetric imaging. The frequency of operation is 0.75 MHz – 3 MHz. The element periodicity was 420 μm. This limits the element size to 400 μm by 400 μm. 76 membranes of 36 μm diameter were used. The physical dimensions of the through-wafer via are shown in Fig. 11. Although it was not possible to test all of the 16384 elements to determine the yield, we were able to test a 128 element sub-array, all of which worked.

VI. Conclusion

This paper is a review of the CMUT process in view of the functional yield. We described the current CMUT process by comparing it to the older versions. We discussed the improvements that the changes will make, and finally demonstrated these on real cases. We increased our functional yield to 100 % which made the imaging experiments with fully functional 1D and 2D arrays possible. The imaging experiments done with these arrays are presented and discussed in another paper in this conference [18].

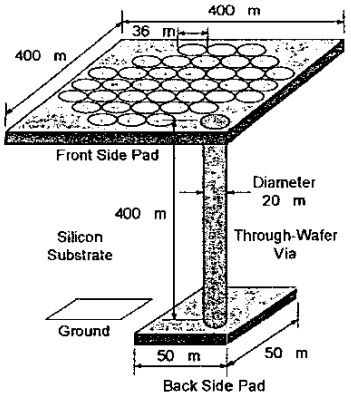


Fig. 11: A schematic view of a 2D array element with a through wafer interconnect.

REFERENCES

[1] M. Haller and B.T. Khuri-Yakub, "A surface micromachined electrostatic ultrasonic air transducer," in Proc. Ultrason. Symp., p. 1241-1244, 1994.

[2] M. Haller and B. T. Khuri-Yakub, "A Surface Micromachined Electrostatic Ultrasonic Air Transducer," IEEE T Trans. Ultrason, Freq. Contr., vol. 43, p. 1-6, January 1996.

[3] H. T. Soh, I. Ladabaum, A. Atalar, C. F. Quate and B. T. Khuri-Yakub, "Silicon Micromachined Ultrasonic Immersion Transducers", Applied Physics Letters, vol. 69, p. 3674-3676, December 1996

[4] D.W. Schindel, D.A. Hutchins, L. Zhoou, and M. Sayer, "The design and characterization of micromachined air coupled capacitance transducers," IEEE Trans. Ultrason, Freq. Contr., vol. 42, p. 42-50, May 1995

[5] I. Ladabaum, X.C. Jin, H.T. Soh, A. Atalar, and B.T. Khuri-Yakub, "Surface micromachined capacitive ultrasonic transducers ," IEEE Trans. Ultrason, Freq. Contr., vol. 45, p. 678-690, May 1998.

[6] X.C. Jin, I. Ladabaum abd B. T. Khuri-Yakub. "The Microfabrication of Capacitive Ultrasonic Transducers", IEEE J. Microelectromechanical Systems., vol. 7, no. 3 p. 295-302, September 1998.

[7] X.C. Jin, I. Ladabaum, L. Degertekin, S. Calmes, and B.T. Khuri-Yakub, "Fabrication and characterization of surface micromachined capacitive ultrasonic transducers," IEEE J. Microelectromechanical Systems., vol. 8(1), p. 100-114, March 1999.

[8] A. G. Bashford, D.W. Schindel, and D.A. Hutchins "Micromachined ultrasonic capacitance transducers for immersion applications," in IEEE Trans. Ultrason, Freq. Contr., vol. 45, p.367-375, Mar. 1998.

[9] X.C. Jin, Ö. Oralkan, F. Levent Degertekin, and Butrus T. Khuri-Yakub, "Characterization of One-Dimensional Capacitive Micromachined Ultrasonic Immersion Transducer Arrays, " IEEE Trans. on UFFC, vol 48, pp. 750-760, May 2001.

[10] Ö. Oralkan, X.C. Jin, F. L. Degertekin, and B.T. Khuri-Yakub, "Simulation and Experimental Characterization of a 2-D Capacitive Micromachined Ultrasonic Transducer Array Element," IEEE Trans. on UFFC vol. 46, pp. 1337-1340, November 1999.

[11] O. Oralkan, X. C. Jin, K. Kaviani, A. S. Ergun, F. L. Degertekin, M. Karaman, and B. T. Khuri-Yakub, "Initial Pulse-Echo Imaging Results with One-Dimensional Capacitive Micromachined Ultrasonic Transducer Arrays," IEEE Ultrasonics Symposium Proceedings, pp. 959-962, 2000.

[12] C. H. Cheng, A. S. Ergun and B. T. Khuri-Yakub, "Electrical Through-Wafer Interconnects with 0.05 Picofarads Parasitic Capacitance on 400 μm Thick Silicon Substrate", Solid-State Sensor, Actuator and Microsystems Workshop, Hilton Head 2002, p. 157-160

[13] C. H. Mastrangelo, C. H. Hsu, "Mechanical Stability and Adhesion of Microstructures Under Capillary Forces – Part I : Basic Theory", IEEE Journal of Microelectromechanical Systems, vol. 2, no. 1, p. 33-43, March 1993.

[14] C. H. Mastrangelo, C. H. Hsu, "Mechanical Stability and Adhesion of Microstructures Under Capillary Forces – Part II : Experiments", IEEE Journal of Microelectromechanical Systems, vol. 2, no. 1, p. 44-55, March 1993.

[15] N. Tas, T. Sonnenberg, H. Jansen, R. Legtenberg, M. Elwenspoek, "Stiction in surface micromachining", Journal of Micromech. Microeng., vol. 6, p. 385-397, 1996.

[16] Ayhan Bozkurt, Igal Ladabaum, Abdullah Atalar, and Butrus T. Khuri-Yakub, "Theory and Analysis of Electrode Size Optimization for Capacitive Microfabricated Ultrasonic Transducers", IEEE Trans. on UFFC vol. 46, pp. 1364-1374, November 1999.

[17] F. V. Hunt, in Electroacoustics, 2nd ed., American Institute of Physics., 1982

[18] O. Oralkan, A. S. Ergun, C. H. Cheng, J. A. Johnson, M. Karaman, B.T. Khuri-Yakub, "Underwater Acoustic Imaging Using Capacitive Micromachined Ultrasonic Transducer Arrays", in press, Oceans 2002, Biloxi, Mississippi, October 2002.