Electrical Through-Wafer Interconnects with Sub-PicoFarad Parasitic Capacitance

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***Abstract*-This paper presents a technology for high density and low parasitic capacitance electrical through-wafer interconnects to an array of capacitive micromachined ultrasonic transducers (CMUTs) on a silicon wafer. Vertical wafer feedthroughs (interconnects) connect an array of sensors or actuators from the front side (transducer side) to the backside (packaging side) of the wafer. A 20 to 1 high aspect ratio 400 μm long and 20 μm diameter interconnect is achieved by using deep reactive ion etching (DRIE). Reduction of the parasitic capacitance of the polysilicon pads to the substrate can be achieved by using reversed-biased pn-junction diodes operating in the depletion region. A parasitic capacitance of 0.3 pF has been achieved by this means. This three-dimensional architecture allows for elegant packaging through simple flip-chip bonding of the chip's back side to a printed circuit board (PCB) or a signal processing wafer.**

I. Introduction

One of the main problems in fabricating two-dimensional ultrasonic transducer arrays is the addressing of the individual array elements [1][2][3]. If the array size is large, a significant sacrifice in the array element area is required if the addressing is done through a routing network. Although ultrasonic transducers are considered here, this problem is a challenge for any kind of array fabrication. This paper presents a solution with technology that provides electrical interconnects to arrays of micro-electro mechanical systems (MEMS) devices on a silicon wafer.

The architecture is based on through-wafer vertical interconnects with high aspect ratio. Many processes have been previously used to fabricate through-wafer interconnects [4][5] including dry etched polysilicon filled interconnects by Chow et al [6]. For our previous work, we have integrated similar interconnects into an active sensor array and made improvements on a parasitic capacitance of 2.67 pF [7].

In an ultrasonic transducer array operation, the parasitic capacitance of the interconnect between an array element and its electronics is the limiting factor for the dynamic range and frequency bandwidth. Therefore, it is always best to put the electronics as close to the array elements as possible. In this work, we demonstrate a way to integrate a 128 x 128 capacitive micromachined ultrasonic transducer (CMUT) array with the electronic circuits without sacrificing the performance of either one and minimizing the parasitic capacitance. To do this, an electrical through-wafer interconnect (ETWI) is employed to address the array elements individually (Fig. 1), where the front side of the wafer is fully populated with the ultrasonic array elements, and the backside is solely dedicated to bond pads for the flip-chip bonding to the printed circuit board (PCB) or the integrated circuits (Fig. 1). In this way, the parasitics due to any interconnection cable are avoided. To further improve the device performance, the parasitic capacitance of the ETWI to the silicon substrate needs to be reduced to a comparatively lower level than the device capacitance.

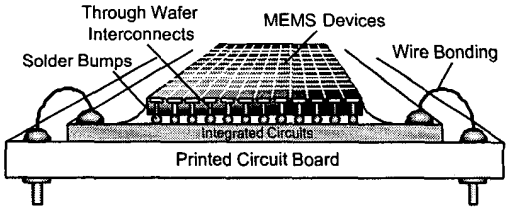

Fig. 1. Packaging schematics of through-wafer interconnects.

II. Parasitic Capacitance Reduction

Parasitic capacitance has a detrimental effect on the performance of the CMUT. For each array element, there are three sources contributing to the parasitic capacitance, the front side 400 μm x 400 μm pad for the bottom electrode of the transducers, the backside 200 μm x 140 μm pad for bonding, and the through-wafer interconnect with 400 μm length and 20 μm diameter (Fig. 2). The optimum solution for the parasitic capacitance reduction is to implement reverse-biased pn-junction diodes on the front and backside pads of the wafer and reverse-biased metal-insulator-semiconductor (MIS) junction inside the interconnects as shown in Fig. 3. Since the silicon substrate is ground, the pads and the through-wafer interconnects have a capacitance with related to the substrate. When the pn junction is applied with a reversed DC bias, the high resistivity (> 1000 ohm-cm) silicon substrate is fully depleted from electrons, thus a low parasitic capacitance is achieved.

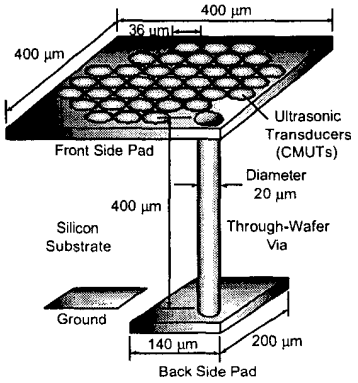

Fig. 2. pn- junction through wafer interconnect schematics.

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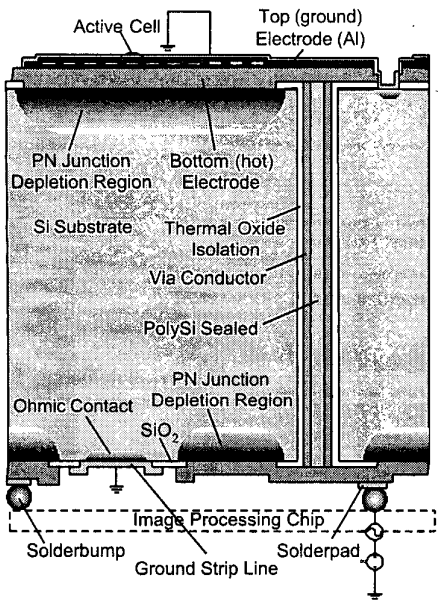

Fig. 3. pn-junction through wafer Interconnect cross section.

III. Expected Parasitic Capacitance

Based on the simulation (Fig. 4), a silicon substrate with resistivity of 1000 ohm-cm is used. A reversed bias voltage of 50 volts is applied to drive the pn-junction diodes into the depletion region. The calculated pn-junction depletion region length is 119 μm. Although the MIS through-wafer interconnect depletion region length is only 9.26 μm, the depletion region of the pn-junction pads can also spread into the substrate near the through-wafer interconnect that the parasitic capacitance of the through-wafer interconnect is further reduced on the regions near both pads. We expect a total parasitic capacitance of 0.234 pF including the front and back side pads and a single through-wafer interconnect which is a substantial improvement compared to the previous result reported [7].

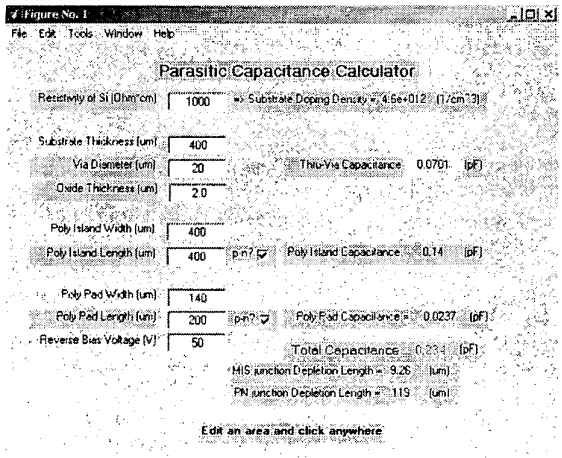

Fig. 4. Expected parasitic capacitance.

IV. Through Wafer Intrconnect Process

The process flow is shown in Fig. 5. We start with a 400 μm thick double-sided polished n-type <100> Si wafer which is thermally oxidized to 2 μm thick to serve as a hard mask for the deep etch. Both sides are then patterned with 20 μm diameter openings for each interconnect. The through-wafer deep etch is done by etching half way from both sides of the wafer (Fig. 5a). By this means, a 20 to 1 high aspect ration via hole can be achieved. When the interconnect is etched through, the helium flow used for cooling goes through the etched holes, and the etching will be slowed down, serving as an etch stop. The oxide mask is then removed by buffered oxide etch (BOE). For MIS isolation at locations with no pn junction, the wafer is thermally oxidized to 1 μm (Fig. 5b). A layer of 2 μm polysilicon is deposited and then heavily doped with boron to enhance the conductance (Fig. 5c). A layer of low temperature oxide (LTO) is deposited to serve as an etching stop for the etch-back of polysilicon deposited in the following step. The interconnect holes are then filled with polysilicon (Fig. 5d). The polysilicon on both sides is then etched back and stopped on the LTO (Fig. 5e). After removing the LTO, the 2 μm doped polysilicon is exposed again and ready to be etched for the front and back side oxide opening (Fig. 5f). Another layer of 0.5 μm polysilicon is deposited and doped with boron which makes up the pn junctions (Fig. 5g). The front and back side polysilicon pads are patterned followed by the oxide etch on the back side for ground opening and heavily doped for ohmic contact. After this step, the ultrasonic transducers (CMUTs) can be built on top of the front side polysilicon (Figs. 6 and 7). At the very end, the back side metal pads for flip-chip bonding are formed by lift-off (Fig. 8). The SEM pictures show the cross section of a finished interconnect in Fig. 9. The wafer is ready for flip-chip bonding to a circuit chip or PCB.

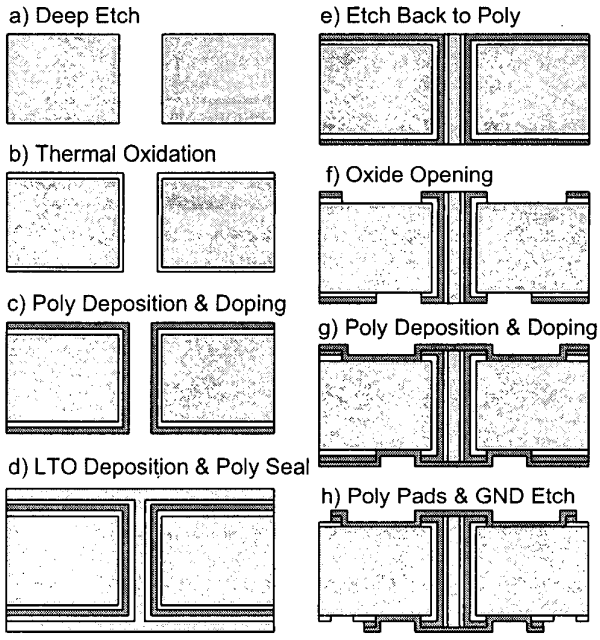

Fig. 5. Fabrication process for through-wafer interconnects.

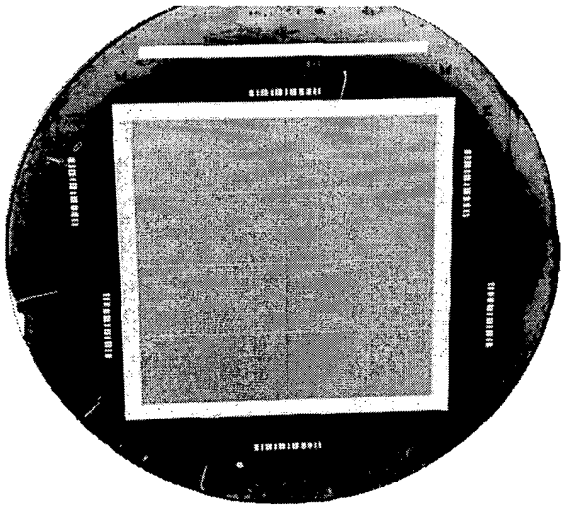

Fig. 6. Photograph of a finished 128 x 128 CMUT array on a 4" silicon wafer.

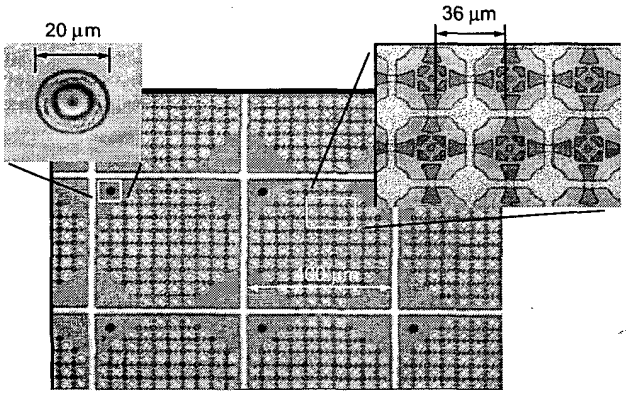

Fig. 7. Photograph of the CMUT array elements with interconnects.

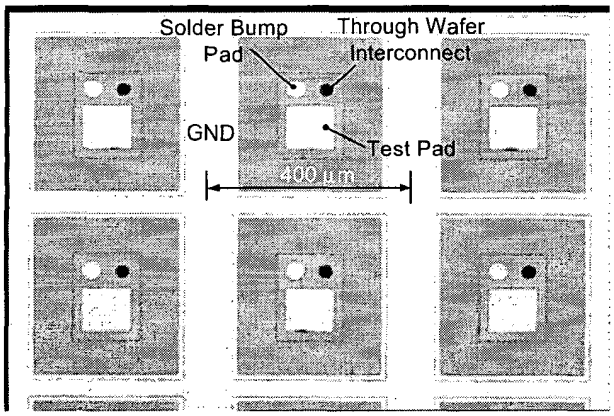

Fig. 8. Photograph of the wafer backside.

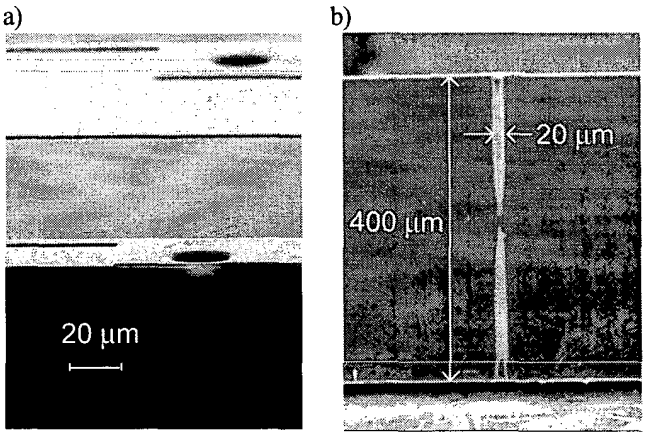

Fig. 9. SEM picture of the cross section of the interconnects.

V. Test Results

A. C-V Characterization of Through-Wafer Interconnects with PN-Junction Pads

As shown in Fig. 10, a testing device with a through-wafer interconnect connected with both front side and back side pads and a ground to the substrate is employed to measure the C-V characteristic at 1 MHz frequency. A reversed DC bias is applied to drive both pn-junction pads into the depletion region. The total capacitance is the capacitance of the through-wafer interconnect plus both pads.

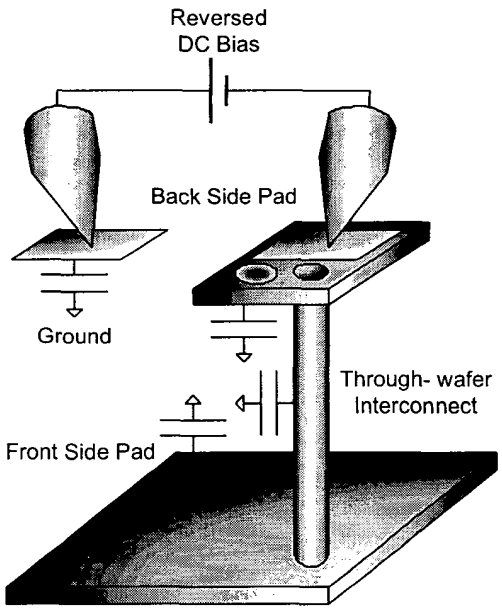

Fig. 10. Capacitance measurement set-up.

Fig. 11 shows a C-V characteristics at 1 MHz frequency. By applying a reverse bias for more than 5 volts the capacitance will decrease to 0.3 pF because of depletion into the substrate. This experimental result is very close to what we expected from the simulation.

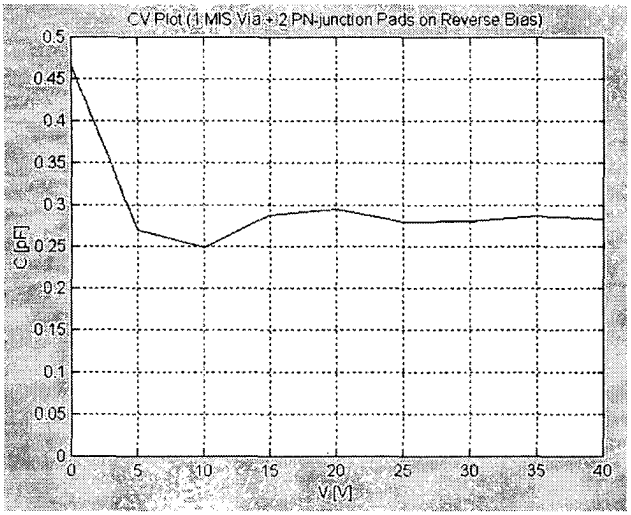

Fig. 11. Measured C-V curve of through-wafer interconnects

B. Impedance Measurement of CMUTs with Interconnects

The experimental setup is similar to that of the CV measurement but with integrated CMUTs on the front side pad. Fig. 12 shows the input impedance of a CMUT array element connected to the wafer back side with an interconnect operating at 20 volts applied bias. The acoustical resonance behavior of the CMUT shows that the through-wafer interconnects are indeed working. However, note that there is a baseline of around 130 ohm in the impedance characteristic which is due to the series resistance of the through-wafer interconnects.

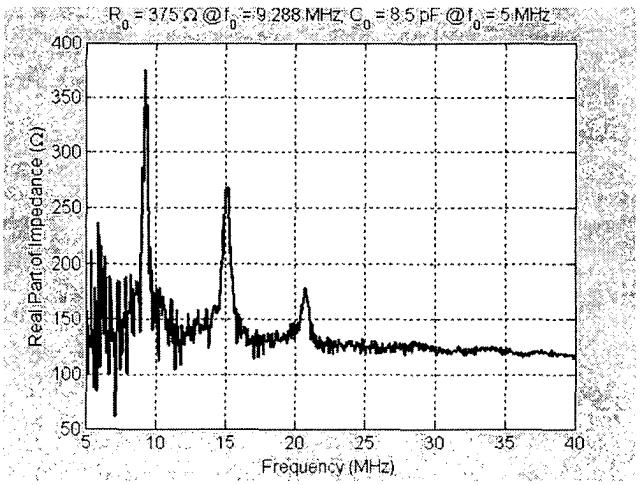

Fig. 12. Impedance measurement of CMUTs with through -wafer interconnects.

VI. Conclusion

Both C-V and impedance measurements reveal that electrical through-wafer interconnects with very low parasitic capacitance have been achieved. Although the series resistance of the through-wafer interconnects is not very serious for the CMUT application, it stands as a problem for the future. This series resistance can be substantially reduced by employing multiple polysilicon deposition and boron doping cycles at step c of Fig. 5 which will be shown in a future work.

Acknowledgment

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