AN EFFICIENT ELECTRICAL ADDRESSING METHOD USING THROUGH-WAFER VIAS FOR TWO-DIMENSIONAL ULTRASONIC ARRAYS

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Abstract - This paper presents a technology for high density and low parasitic capacitance electrical interconnects to arrays of Capacitive Micromachined Ultrasonic Transducers (CMUTs) on a silicon chip. Vertical wafer feedthroughs (vias) connect an array of sensors or actuators from the front side (transducer side) to the backside (packaging side) of the chip. A 20 to 1 high aspect ratio 20 μm diameter via is achieved by using Deep Reactive Ion Etching (DRIE). Reduction of the parasitic capacitance of the polysilicon pads to the substrate can be achieved by using Metal Insulator Semiconductor (MIS) operating in the depletion region. This three-dimensional architecture allows for elegant packaging through simple flip-chip bonding of the chip's back side to a printed circuit board (PCB) or a signal processing chip.

I. INTRODUCTION

One of the main problems in fabricating two dimensional ultrasonic transducer arrays is the addressing of the individual array element [1][2][3]. If the array size is large, a significant sacrifice in the array element area is required if the addressing is done through a routing network. Although ultrasonic transducers are considered here, this problem is a challenge for any kind of array fabrication. This paper presents a solution with technology that provides electrical contacts to arrays of MEMS devices on a silicon chip.

The architecture is based on through-wafer vertical vias with high aspect ratio. Many processes have been previously used to fabricate through-wafer interconnects [4][5] including dry etched polysilicon filled interconnects by Chow et al [6]. This work integrates similar interconnects into an active sensor array and makes improvements in achievable capacitance. Compared with our previous two-dimensional array work [2], this interconnects technology demostrated lower parasitic capacitance with ease in doing standard photolithography instead of using dry film photoresist. Bringing the contacts to the backside of the wafer allows for efficient, elegant, and compact packaging through flip-chip bonding to a PCB or signal processing chip. The front side of the wafer can be dedicated solely to the active devices, maximizing their efficiency, whereas the backside contains the flip-chip connection. In this way we have been able to fabricate a 128 x 128 array with an array element size of 420 μm x 420 μm. Reduction of both the parasitic capacitance and leakage current of the pads on both sides and the through-wafer via is the main issue in optimizing the fabrication process. The optimum solution for these interconnects is reverse-biased pn-junction diodes on the front and back sides of the wafer, and a reverse-biased Metal Insulator Semiconductor (MIS) junction inside the via. In this way, it is possible to reduce the parasitic capacitance into the sub-picofarad range. An alternative solution is used in this paper by applying MIS on both pads and vias. The front side of the wafer is fully populated with the ultrasonic array elements, where the backside contains only a small pad for flip-chip bonding.

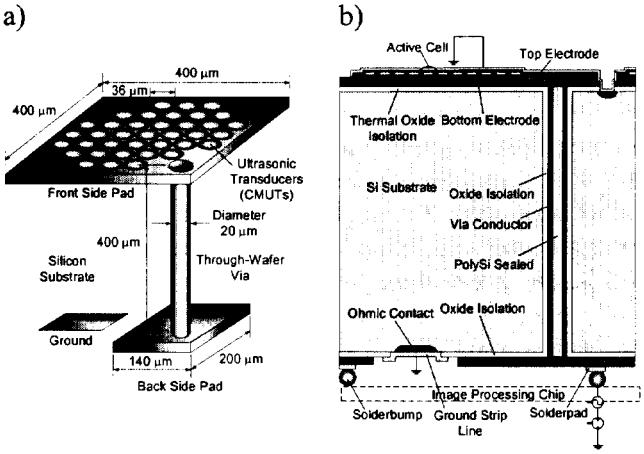

Figure 1. a) MIS through wafer via schematics
b) MIS through wafer via cross section.

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II. DEVICE CONSIDERATIONS

Parasitic capacitance has a detrimental effect on the performance of the CMUT. As shown in Figure 1a, the parasitic capacitance comes about from the 400 μm x 400 μm front side pad, the 200μm x 140μm back side pad, and the 20 μm diameter by 400 μm long through-wafer via that connects the two pads. The front side pad contributes most of the parasitic capacitance. For an MIS device, the capacitance is decreased by operating the device in the depletion region at high frequency. A very low doping concentration substrate is used to increase the depletion depth that results in a decrease of the capacitance (Fig. 1b). To further reduce the parasitic capacitance, a pn junction front side pad will be used that will be discussed in the paragraph of future work.

III. Through-Wafer Via Process

The process flow is shown in Fig. 2. We start with a 400 μm thick double-sided polished n-type <100> Si wafer which is thermally oxidized to 2 μm thick to serve as a hard mask for the deep etch. Both sides are then patterned with 20 μm diameter openings for each via. The through-wafer deep etch is done by etching half way from both sides of the wafer (Fig. 2a). By this means, a 20 to 1 high aspect ration via hole can be achieved. When the via is etched through, the helium flow used for cooling goes through the etched holes, and the etching will be slowed down, serving as an etch stop. The oxide mask is then removed by buffered oxide etch (BOE). For MIS isolation, via side walls and wafer front and backside pads are grown with 1 μm of thermal oxide (Fig. 2b). A layer of 2 μm polysilicon is deposited and then heavily doped with phosphorous to enhance the conductance (Fig. 2c). A layer of low temperature oxide (LTO) is deposited to serve as an etching stop for the etch-back of polysilicon deposited in the following step. The via holes are then filled with polysilicon (Fig. 2d). The polysilicon on both sides is then etched back and stopped on the LTO (Fig. 2e). After removing the LTO, the 2 μm doped polysilicon is exposed again and ready to be etched for the front and back side pads patterning (Fig. 2f). The oxide is opened on the back side for ground opening and heavily doped for ohmic contact The SEM pictures show the cross section of a finished via in Fig. 3. After this step, the ultrasonic transducers (CMUTs) can be built on top of the front side polysilicon (Fig. 4). At the very end, the back side metal pads for flip-chip bonding are formed by lift-off. The wafer is ready for flip-chip bonding to a circuit chip or PCB.

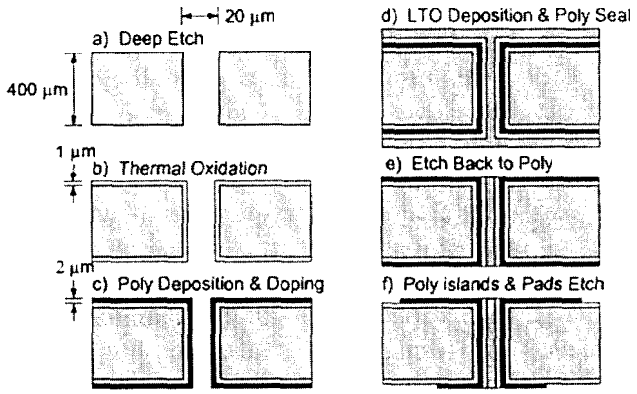

Figure 2. Fabrication Process for a through-wafer via.

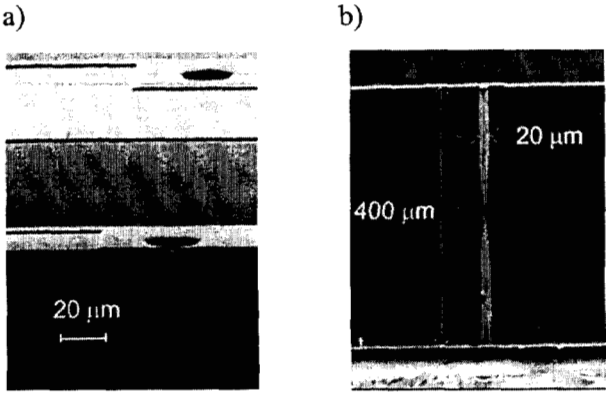

Figure 3. SEM picture of the cross section of the via.

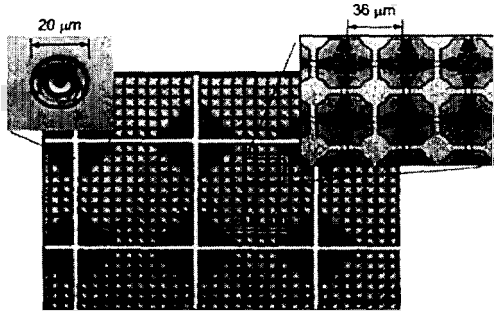

Figure 4. Photograph of the transducers with vias.

IV. TESTING RESULTS

I-V Characterization of Continuity for Through-Wafer Vias with MIS Pads

A testing device with two through-wafer vias connected with a pad on the front side and two pads on the backside is employed to obtain I-V characteristics of the via continuity.

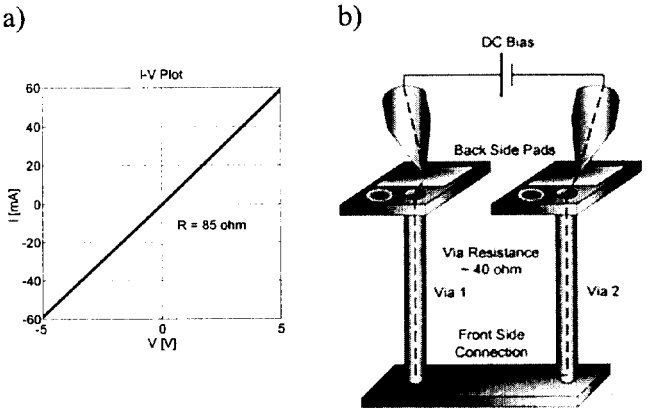

Figure 5. Electrical continuity test set-up.

As shown in Fig. 5, this is a pure resistor with a resistance of 85 Ω. The resistance of one via is thus around 40 Ω, which is satisfactory for the ultrasonic transducer application.

I-V Characterization of Isolation for Through-Wafer Vias with MIS Pads

A testing device with two through-wafer vias isolated with a layer of thermal oxide grown on the silicon substrate is employed to obtain I-V characteristics of the via isolation.

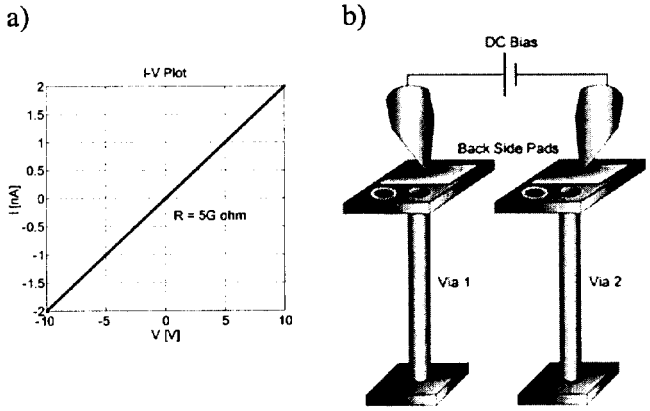

Figure 6. Isolation test set-up.

As shown in Figure 6, the leakage current at 10 volts is only 2 nA and the resistance is 5 GΩ. This means via isolation is sufficient for our application.

C-V Characterization of Through-Wafer Vias with MIS Pads

A testing device with a through-wafer via connected with both front side and back side pads and a ground to the substrate is employed to measure the C-V characteristic. The total capacitance is the capacitance of the via plus both pads.

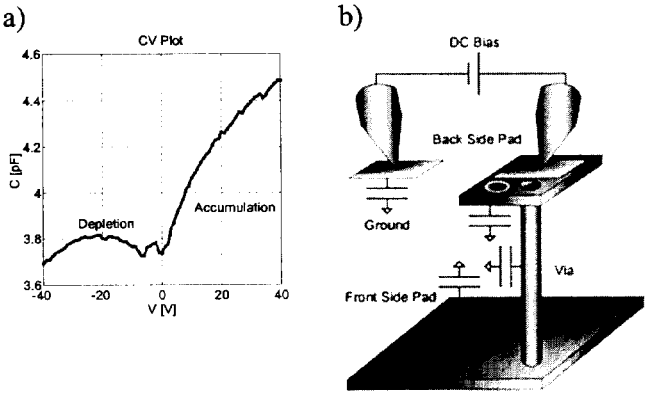

Figure 7. Capacitance measurement set-up.

Figure 7 shows a MIS C-V characteristics at 1 MHz frequency. By applying a reverse bias, the capacitance will decrease because of depletion into the substrate.

Impedance Measurement of CMUTs with Vias with MIS Pads

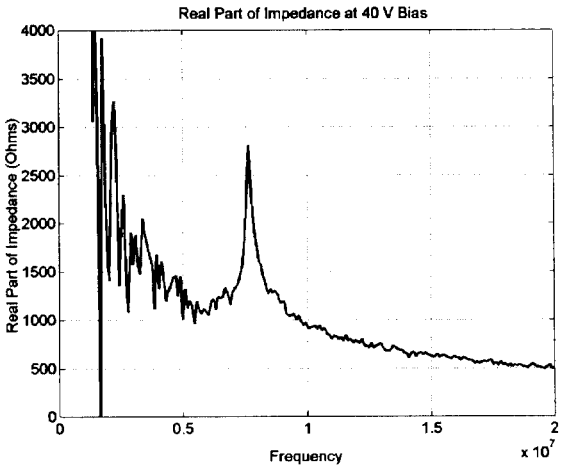

Figure 8. Impedance of CMUTs with Vias.

The experimental setup is similar to that of the CV measurement but with integrated CMUTs on the front side pad. Figure 8 shows the input impedance of a CMUT array element connected to the wafer back side with a via operating at 40 volts applied bias. The resonance frequency is at 7.5 MHz. We obtained a 3.76 pF total capacitance which corresponds to a 2.76 pF parasitic capacitance by subtracting the 1 pF capacitance of the CMUT.

V. FUTURE WORK

Most of the parasidic capacitance is contributed by the front side 400 μm x 400 μm pad. In order to reduce the parasitic capacitance, the front side and back side pads need to be depleted to the substrate by using pn junction devices. As shown in Fig. 8, there are oxide openings on both sides for the pn junction devices. Simulation predicts the total parasitic capacitance can be reduced to 1.5 pF.

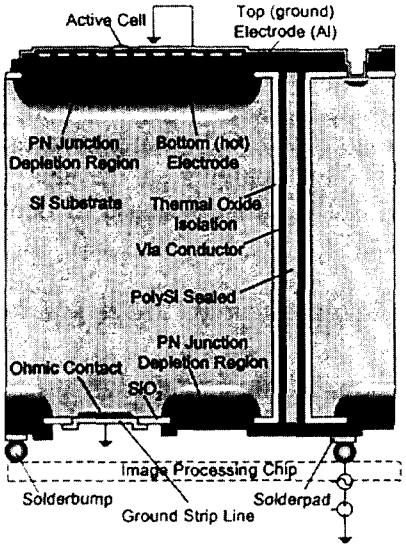

Figure 8

VI. CONCLUSIONS

A two-dimensional ultrasonic transducer array with through-wafer vias have been achieved. According to the testing results, the ultrasonic transducers with vias work at our designed frequency 7.5 MHz with an achieved a parasitic capacitance of 2.76 pF. Currently we are optimizing device performance by improving the transducer design and integrating PN junctions under the pads.

VII. ACKNOWLEDGEMENT

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