An Analytical MOS Device Model with Mismatch and Temperature Variation for Subthreshold Circuits

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***Abstract*—Subthreshold analog circuits are attractive for low-power, large-scale neuromorphic systems. However, subthreshold currents are exponentially sensitive to temperature and device mismatch, and a compact model that accounts for these effects is needed. We develop an analytical compact model with mismatch and temperature variation for subthreshold MOS devices. The model only requires an initial set of Monte Carlo (MC) simulations on individual devices for parameter extraction. Then the designer can use its parameterized analytical expressions for circuit design, instead of running repeated MC simulations on large circuits. We apply this model to a subthreshold current mirror design example. Good agreement between the developed model and Spectre simulations is achieved in a 28-nm fully-depleted silicon-on-insulator (FDSOI) process. The model is general and can also guide the design of other subthreshold circuits, such as low-power silicon neurons. It has been used to design Braindrop, the first neuromorphic chip programmed at a high level of abstraction.**

***Index Terms*—CMOS, fully-depleted silicon-on-insulator (FD-SOI), integrated circuit, neuromorphic engineering, semiconductor device modeling, subthreshold, weak inversion.**

I. Introduction

BRAIN-inspired systems are promising approaches for energy-efficient computing [1]. Neuromorphic mixed-analog-digital systems typically have large networks of ultra-low power analog circuit instances [2], [3], [4]. These analog circuits, however, are sensitive to ambient temperature and device mismatch, especially when operating in subthreshold regime [5], [6], [7]. This sensitivity can be compensated at the circuit level (individual neuron circuits) and at the system level (a network of neurons). Compensating at the circuit level generally results in larger area [8], [9], which is undesirable for large-scale systems. Compensating at the system level typically requires knowledge of the analog instances' behaviors (e.g., neurons' input-output curves) in order to configure the system correctly [5], [10]. During the design phase, this characterization is obtained from computationally expensive Monte Carlo (MC) *SPICE* simulations, which are time-consuming. To avoid such tedious simulations and provide additional design insight, compact device models that capture the effect of temperature and device mismatch are needed.

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Existing compact device models of subthreshold operation do not provide a simple analytical relationship that accounts for both drain-current mismatch and temperature [11], [12], [13]. To address this, we develop a physics-based analytical MOS device model with just seven parameters. This model saves the designer from repeatedly running tedious MC simulations on the complete circuits. This compact device model was used to design Braindrop [14], the first neuromorphic chip programmed at a high level of abstraction. We sought to develop a compact model that achieves $\pm 10\%$ accuracy in the commercial temperature range (0–70°C).

In Section II, we present our compact device model. In Section III, we perform parameter extraction. In Section IV, we illustrate how to use the device model to predict a current mirror's sensitivity to temperature and mismatch and compare these predictions with Cadence Spectre simulations. We provide concluding remarks in Section V.

II. Device Model for Mismatch and Temperature

In this section, we develop a compact MOS device model that captures the effect of mismatch and temperature variations in the subthreshold regime. The developed model is general and can be useful for any subthreshold MOS circuit where temperature and mismatch matter, which encompasses the majority of practical designs.

A. Threshold Voltage Variation with Temperature

An NMOS transistor's drain current, I_D, in weak inversion (subthreshold) can be modeled as [11], [12], [15], [16]

$$I_D = \frac{W}{L} C'_{\rm ox} \left(\kappa^{-1} - 1\right) e^1 U_T^2 \, b \, T^{-\alpha} e^{\frac{(1-\kappa)V_{\rm BS}}{U_T}} \times e^{\frac{\kappa(V_{\rm GS}-V_t)}{U_T}} e^{\lambda \Delta V_{\rm DS}} \left(1 - e^{-\frac{V_{\rm DS}}{U_T}}\right), \quad (1)$$

where W and L are the width and length of the device, respectively; $C'_{\rm ox}$ is the oxide capacitance per unit area; κ is the subthreshold slope factor; $U_T \equiv kT/q$ is the thermal voltage; $bT^{-\alpha}$ models electron mobility; $V_{\rm t}$ denotes the threshold voltage; and λ models the combined effect of drain-induced barrier lowering (DIBL) and channel-length modulation (CLM). $V_{\rm GS}$, $V_{\rm BS}$ and $V_{\rm DS}$ are the gate, bulk and drain voltages, respectively, relative to source voltage; and $\Delta V_{\rm DS} = V_{\rm DS} - V_{\rm DS_{ref}}$, where $V_{\rm DS_{ref}}$ is a reference voltage. We now rewrite (1) as

$$I_D(T) = \frac{W}{L} C'_{\rm ox} \left(\kappa^{-1} - 1\right) e^1 \frac{k^2}{q^2} \, b \, T_{\rm nom}^{2-\alpha} \, e^{-\frac{\kappa V_{\rm t}^*}{U_T}} e^{\frac{(1-\kappa)V_{\rm BS}}{U_T}} \times e^{\frac{\kappa V_{\rm GS}}{U_T}} e^{\lambda \Delta V_{\rm DS}} \left(1 - e^{-\frac{V_{\rm DS}}{U_T}}\right), \quad (2)$$

where

$$V_{\mathrm{t}}^{*} = \frac{U_T}{\kappa}\,(\alpha-2)\log\left(\frac{T}{T_{\mathrm{nom}}}\right) + V_{\mathrm{t}}. \tag{3}$$

We introduce V_{t}^{*}, to combine process-specific terms that strongly affect I_D's temperature dependence and mismatch, which will later be used for the mismatch analysis. T_{nom} is the nominal temperature. The threshold voltage V_{t} for an FDSOI device can be modeled as [17]

$$V_{\mathrm{t}} = \phi_{\mathrm{m}} + U_T \log\left(\frac{2\,C'_{\mathrm{ox}}\,U_T}{n_{\mathrm{i}}\,q\,t_{\mathrm{Si}}}\right) + \frac{\pi^2\hbar^2}{2\,q\,m^{*}\,t_{\mathrm{Si}}^2}, \tag{4}$$

where ϕ_{m} is the metal gate's work-function with respect to that of intrinsic silicon, q is the electronic charge, n_{i} is the intrinsic carrier concentration, t_{Si} is the silicon channel's thickness, $\hbar$ is the Dirac constant and m^{*} is the charge carrier's confinement mass in the transverse direction. n_{i}'s and ϕ_{m}'s temperature dependence [18], [19] can be modeled as

$$n_i\,(T) = \; b_0\left(\frac{T}{T_{\mathrm{nom}}}\right)^{b_1} e^{-\frac{b_2}{T}} \text{ and } \phi_{\mathrm{m}}\,(T) = \; c_0 T + c_1 \tag{5}$$

to first order. From (4) and (5), we arrive at

$$\begin{aligned}\frac{\kappa V_{\mathrm{t}}^{*}}{U_T} = \; & \kappa\log\left(\frac{2\,C'_{\mathrm{ox}}k}{b_0\,q^2\,t_{\mathrm{Si}}}\right) + (\kappa\,b_1 + 2 - \alpha)\log\left(T_{\mathrm{nom}}\right) \\ & + \frac{\kappa\,q}{k}c_0 + \kappa\left(b_2 + \frac{q\,c_1}{k} + \frac{\pi^2\,\hbar^2}{2k\,m^{*}\,t_{\mathrm{Si}}^2}\right)\frac{1}{T} \\ & + ((b_1-1)+2-\alpha)\log\left(\frac{1}{T}\right). \end{aligned} \tag{6}$$

Neglecting $\log(1/T)$'s contribution and grouping the first three terms on the right-hand side (which do not depend on temperature) as γ_2, we simplify (6) to

$$\frac{\kappa V_{\mathrm{t}}^{*}}{U_T} = \; \gamma_1\frac{T_{\mathrm{nom}}}{T} + \gamma_2, \tag{7}$$

as our approximation for V_{t}^{*}'s temperature dependence, where

$$\gamma_1 = \kappa\left(b_2 + \frac{q\,c_1}{k} + \frac{\pi^2\,\hbar^2}{2k\,m^{*}\,t_{\mathrm{Si}}^2}\right)\frac{1}{T_{\mathrm{nom}}}, \tag{8}$$

$$\gamma_2 = \; \kappa\log\left(\frac{2\,C'_{\mathrm{ox}}k}{b_0\,q^2\,t_{\mathrm{Si}}}\right) + (\kappa\,b_1 + 2 - \alpha)\log\left(T_{\mathrm{nom}}\right) + \frac{\kappa\,q}{k}c_0. \tag{9}$$

B. Device Mismatch Effects on Drain Current Variation

We now derive the effect of device mismatch on the drain current. I_{D} varies between transistors (for the same bias voltages) due to threshold variations that can be written as $V_{\mathrm{t}}^{*} = \langle V_{\mathrm{t}}^{*}\rangle + \Delta V_{\mathrm{t}}^{*}$, where $\langle V_{\mathrm{t}}^{*}\rangle$ is V_{t}^{*}'s mean value and $\Delta V_{\mathrm{t}}^{*}$ is a zero-mean random variable. Therefore, we can rewrite (2) as

$$I_{\mathrm{D}} = \overbrace{e^{-\frac{\kappa\Delta V_{\mathrm{t}}^{*}}{U_T}}}^{\Lambda} I_{\mu} \tag{10}$$

$$I_{\mu}\,(T) \; = I_0\,e^{\frac{(1-\kappa)V_{\mathrm{BS}}}{U_T}} \times e^{\frac{\kappa V_{\mathrm{GS}}}{U_T}}\left(1 - e^{-\frac{V_{\mathrm{DS}}}{U_T}}\right)e^{\lambda\Delta V_{\mathrm{DS}}} \tag{11}$$

$$I_0\,(T) \; = \frac{W}{L}C'_{\mathrm{ox}}\left(\kappa^{-1}-1\right)e^{1}\,\frac{k^2}{q^2}\,b\,T_{\mathrm{nom}}^{2-\alpha}e^{-\frac{\kappa\langle V_{\mathrm{t}}^{*}\rangle}{U_T}} \tag{12}$$

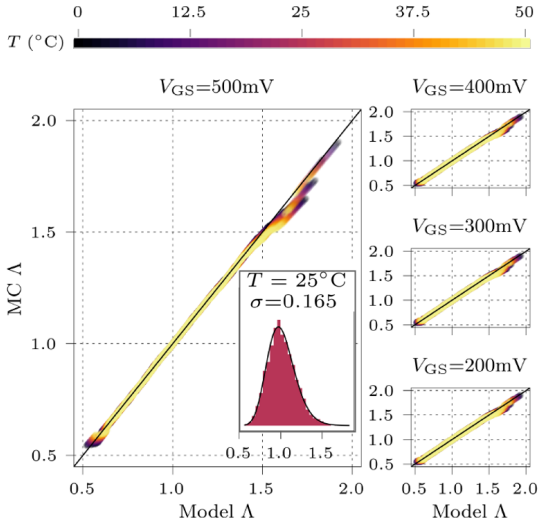

Fig. 1. Current distribution: For a given V_{GS} and T, the current mismatch ($\Lambda = I_{\mathrm{D}}/I_{\mu}$) of 5000 thick-oxide transistor instances (W = 160nm and L = 450nm, 28-nm FDSOI process) biased in the subthreshold regime is distributed approximately Lognormally, as is seen by plotting this distribution (model Λ) vs. the empirical (MC Λ) one. The Lognormal distribution is a good fit across a 300mV range of V_{GS} (200mV to 500mV) and a 50°C range of T (0°C to 50°C), except for its tails, which are inaccurately sampled. Note that the distribution tightens as temperature increases (lighter dots are spread less than darker dots). The inset shows the MC distribution's empirical PDF (red fills) and the best-fit Lognormal (solid line) at 25°C for $V_{\mathrm{GS}} = 500$mV. For all plots, $V_{\mathrm{BS}} = -1$V.

where Λ denotes current mismatch. Note that, in the above model, I_{μ} has no randomness (λ's mismatch is ignored).

In Monte Carlo simulations for various V_{GS}, we observed that $\Lambda = I_{\mathrm{D}}/I_{\mu}$ is Lognormally distributed (see Fig. 1's inset) and that its standard deviation decreases with increasing temperature. We could reproduce this temperature dependence (Fig. 2) by rewriting (7) in the form

$$\frac{\kappa\left(\langle V_{\mathrm{t}}^{*}\rangle + \Delta V_{\mathrm{t}}^{*}\right)}{U_T} = \left(\langle\gamma_1\rangle + \Delta\gamma_1\right)\frac{T_{\mathrm{nom}}}{T} + \langle\gamma_2\rangle + \Delta\gamma_2, \tag{13}$$

where $\langle\gamma_{1,2}\rangle$ are constants and $\Delta\gamma_{1,2}$ are normally distributed random variables. Thus, the current mismatch Λ is given by

$$\begin{aligned}\Lambda = I_{\mathrm{D}}/I_{\mu} &= e^{-\Delta\gamma_1\frac{T_{\mathrm{nom}}}{T} - \Delta\gamma_2} \\ \Delta\gamma_1 &\sim \mathrm{Normal}\,(0,\sigma_1) \\ \Delta\gamma_2 &\sim \mathrm{Normal}\,(0,\sigma_2)\end{aligned} \tag{14}$$

Its underlying normal distribution's standard deviation σ_{T} varies with temperature as

$$\sigma_{\mathrm{T}} = \mathrm{std}\,(\ln\Lambda) \; = \sqrt{\sigma_1^2\left(\frac{T_{\mathrm{nom}}}{T}\right)^2 + \sigma_2^2}\,. \tag{15}$$

C. Final Drain Current Expression

Next, we model the temperature dependence of I_{μ}. Combining (12) and (13) results in

$$I_0\,(T) = I_{0_{\mathrm{nom}}}e^{\langle\gamma_1\rangle\left(1-\frac{T_{\mathrm{nom}}}{T}\right)}. \tag{16}$$

The temperature dependence of channel-length modulation and drain-induced barrier lowering can be modeled as

$$\lambda\,(T) = \lambda_1\frac{T_{\mathrm{nom}}}{T} + \lambda_2. \tag{17}$$

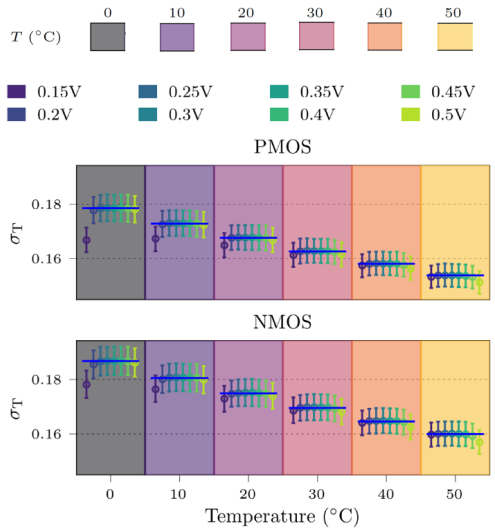

Fig. 2. Current mismatch vs. temperature: $\ln(\Lambda)$'s standard deviation σ_{T} (circles) reduces with increasing temperature (0°C to 50°C) across various V_{GS} (0.15V to 0.5V). This behavior is well captured by our model (blue lines) for both PMOS (top) and NMOS (bottom) devices ($W = 160$nm, $L = 450$nm). Error bars denote 2.5-97.5 percentiles of σ_{T} from 10,000 bootstrap iterations. Notice that, empirically, σ_{T} does not depend strongly on V_{GS}, except for $V_{\mathrm{GS}} = 0.15$V. For these simulations, the bias voltages are set to $V_{\mathrm{DS}} = V_{\mathrm{DS_{ref}}} = \pm 0.5$V, $V_{\mathrm{BS}} = -1$V (NMOS) and 1V (PMOS).

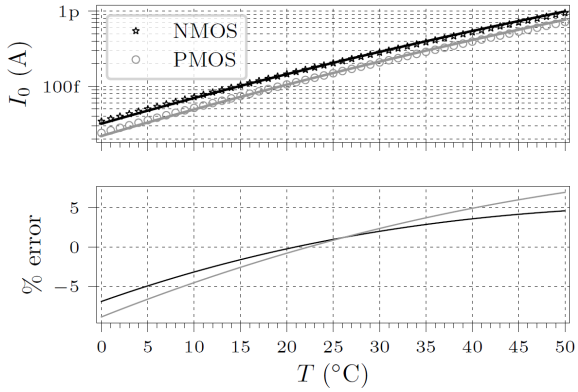

Fig. 3. NMOS' and PMOS' I_0: I_0's temperature dependence obtained from simulation (circles and stars) is well captured by our model's exponential dependence (solid line) for both PMOS and NMOS devices. The bottom panel shows the model's error relative to the simulation results.

This temperature dependence of λ is in agreement with observations from simulations at various V_{DS}. From (11), (16), and (17), I_μ can be written as

$$I_\mu(T) = I_{0_{\mathrm{nom}}} e^{\langle\gamma_1\rangle\left(1-\frac{T_{\mathrm{nom}}}{T}\right)} e^{\frac{(1-\kappa)V_{\mathrm{BS}}}{U_T}} \times e^{\frac{\kappa V_{\mathrm{GS}}}{U_T}} e^{\left(\lambda_1\frac{T_{\mathrm{nom}}}{T}+\lambda_2\right)\Delta V_{\mathrm{DS}}} \left(1-e^{-\frac{V_{\mathrm{DS}}}{U_T}}\right) \quad (18)$$

This equation, together with (14), provide a compact model of the combined effect of temperature and mismatch on a transistor's drain current.

III. Method for Parameter Extraction

In this section, we describe the parameter extraction method. Monte Carlo simulations across temperature and bias voltages are run in Cadence Spectre, for a commercial 28-nm FDSOI process using the UTSOI model [20], [21].

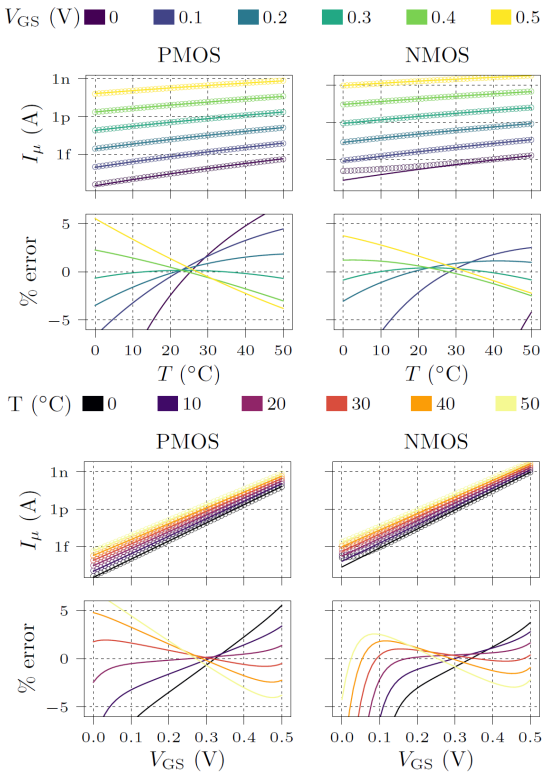

Fig. 4. Drain current for devices without mismatch: I_μ's dependence on T and V_{GS} obtained from simulations (circles) is well captured by our model. I_μ's dependence on T for different V_{GS} values (top half) as well as its dependence on V_{GS} for different T values (bottom half) are shown. The model's error relative to the simulation results (lower panels) is mostly within $\pm 5\%$ for T between 10 and 40°C and V_{GS} between 0.1 and 0.4V.

TABLE I
Parameter values for I_{D}'s temperature and mismatch model

$W = 160$nm	PMOS		NMOS	
L (nm)	450	150	450	150
σ_1	0.156	0.269	0.165	0.286
σ_2	0.0554	0.096	0.049	0.0849
κ	0.792		0.828	
$I_{0_{\mathrm{nom}}}$ (pA)	0.151	1.32	0.205	1.2
$\langle\gamma_1\rangle$	21.0	19.5	20.3	19.0
λ_1	0.212	0.457	0.179	0.39
λ_2	−0.148	−0.0674	−0.135	−0.0638

* Thick-oxide (1.8V) MOS devices are used.
** The long-channel devices ($W = 160$nm, $L = 450$nm) are used in all figures.

There are seven total parameters to fit: two parameters (σ_1 and σ_2) in Λ's model and five parameters (κ, $I_{0_{\mathrm{nom}}}$, $\langle\gamma_1\rangle$, λ_1 and λ_2) in I_μ's model (Table I).

To obtain σ_1 and σ_2, we first run Monte Carlo simulations to acquire I_{D} values from an ensemble of 2500 devices. From these I_{D} values, σ_{T} are determined at each V_{GS} and T (Fig. 2). We then fit σ_{T} to T using (15) to obtain values for σ_1 and σ_2 for each V_{GS}. As the fit parameter values do not vary significantly across the V_{GS} range, except for $V_{\mathrm{GS}} = 0.1$ and 0.5V, we will use their median values in subsequent analysis. We repeat this procedure for $10,000$ ensembles, where each

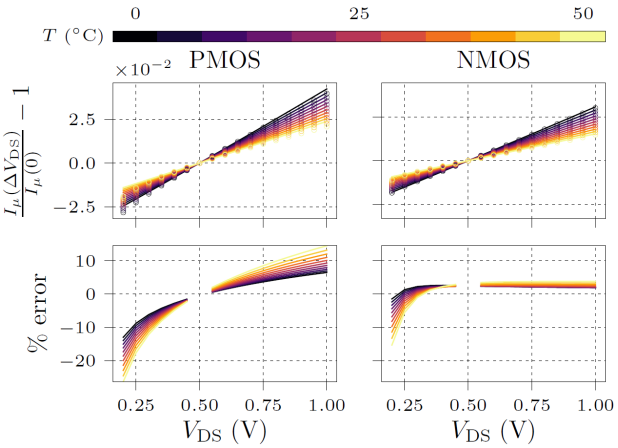

Fig. 5. Drain conductance: Simulated I_{D}'s increase with ΔV_{DS}. I_{D}'s behavior across T (circles) is well matched by our model (solid line) from 0 to 50°C (dark to light colors). The bottom panels show the model's error relative to the simulation results; the error is undefined at $V_{\mathrm{DS}} = V_{\mathrm{DS_{ref}}} = 0.5\mathrm{V}$ because $\Delta V_{\mathrm{DS}} = 0$ for this value of V_{DS}.

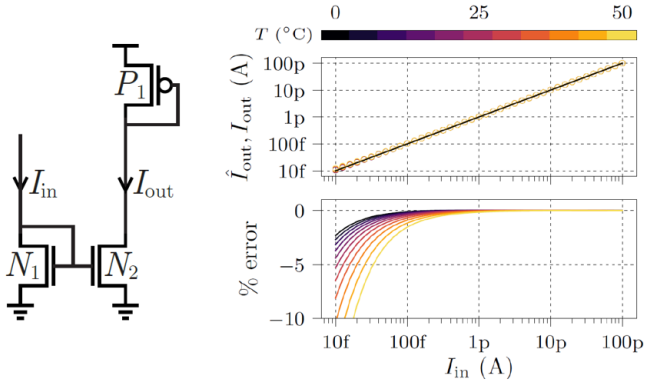

Fig. 6. Current mirror output for devices without mismatch: For an NMOS current mirror circuit feeding a PMOS diode-connected load (left), our model's prediction of output current, $\hat{I}_{\mathrm{out}}$ (solid lines), matches the simulation's, I_{out} (circles), for I_{in} between 100fA and 100pA. Note that $\hat{I}_{\mathrm{out}}$ is less than I_{out} for $I_{\mathrm{in}} < 100\mathrm{fA}$ because N_1 enters the ohmic region, whereas our analysis assumes that all devices are in saturation.

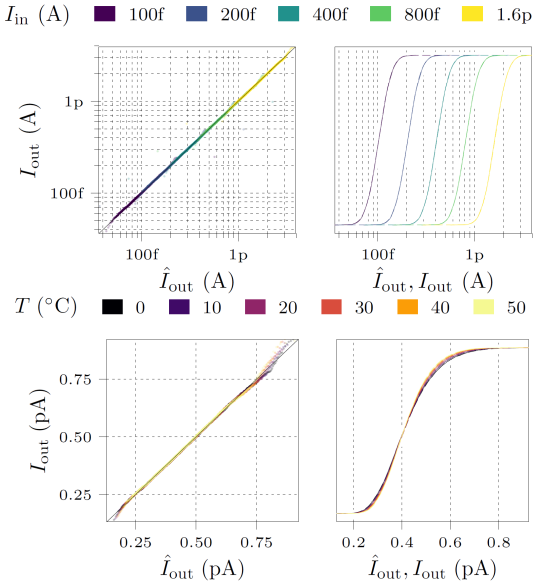

Fig. 7. Current mirror output current: Our model's output current's distribution ($\hat{I}_{\mathrm{out}}$) matches that of a simulated ensemble of 1000 mismatched current mirrors (I_{out}) for different I_{in} values (100fA to 1.6pA) at $T = 25°\mathrm{C}$ (top) and for different T values (0 to 50°C) at $I_{\mathrm{in}} = 400\mathrm{fA}$ (bottom), as seen in their Q-Q (left) and CDF (right) plots; the latter plot uses solid and dashed lines for I_{out} and $\hat{I}_{\mathrm{out}}$, respectively.

ensemble is obtained by randomly selecting, with replacement, 2500 samples from a single pool of 5000 mismatched devices. Using the values from these $10,000$ runs, we calculate σ_1's and σ_2's median and confidence intervals. Obtaining σ_1 and σ_2 means we now have Λ in (10). The modeled and empirical Λ agree closely (Fig. 1).

Fitting I_μ (18) extracts five parameters: $I_{0_{\mathrm{nom}}}$, $\langle\gamma_1\rangle$, κ, λ_1 and λ_2. We first obtain I_{D} values from devices without mismatch at various $V_{\mathrm{GS}} = \pm 0.2 - \pm 0.4\mathrm{V}$, $\Delta V_{\mathrm{DS}} = \mp 0.3 - \pm 0.5\mathrm{V}$ and $T_k = 0 - 50°\mathrm{C}$, for $V_{\mathrm{DS_{ref}}} = \pm 0.5\mathrm{V}$ and for $V_{\mathrm{BS}} = -1\mathrm{V}$ (NMOS) and 1V (PMOS). From these I_{D} values, we estimate the fit parameter values by finding the least squared-error solution to $Ax = y$, where

$$A = \begin{bmatrix} 1 & \frac{T_{\mathrm{nom}}}{T_0} & \frac{V_{\mathrm{GS}_0}}{U_{\mathrm{T_{nom}}}}\frac{T_{\mathrm{nom}}}{T_0} & \Delta V_{\mathrm{DS}_0}\frac{T_{\mathrm{nom}}}{T_0} & \Delta V_{\mathrm{DS}_0} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 1 & \frac{T_{\mathrm{nom}}}{T_k} & \frac{V_{\mathrm{GS}_i}}{U_{\mathrm{T_{nom}}}}\frac{T_{\mathrm{nom}}}{T_k} & \Delta V_{\mathrm{DS}_j}\frac{T_{\mathrm{nom}}}{T_k} & \Delta V_{\mathrm{DS}_j} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 1 & \frac{T_{\mathrm{nom}}}{T_{\mathrm{R}}} & \frac{V_{\mathrm{GS_P}}}{U_{\mathrm{T_{nom}}}}\frac{T_{\mathrm{nom}}}{T_{\mathrm{R}}} & \Delta V_{\mathrm{DS_Q}}\frac{T_{\mathrm{nom}}}{T_{\mathrm{R}}} & \Delta V_{\mathrm{DS_Q}} \end{bmatrix}$$

$$x = \begin{bmatrix} a_0 \\ a_1 \\ \kappa \\ \lambda_1 \\ \lambda_2 \end{bmatrix} \text{ and } y = \begin{bmatrix} \ln I_{\mu_{0,0,0}} \\ \vdots \\ \ln I_{\mu_{i,j,k}} \\ \vdots \\ \ln I_{\mu_{\mathrm{P,Q,R}}} \end{bmatrix} \tag{19}$$

The solutions for a_0 and a_1 yield $I_{0_{\mathrm{nom}}} = e^{a_0 - \langle\gamma_1\rangle}$ and $\langle\gamma_1\rangle = (1-\kappa)\,V_{\mathrm{BS}}/U_{\mathrm{T_{nom}}} - a_1$. With these five parameters extracted, we compare I_0 from (12) and I_μ from (18) to Spectre simulations (Fig. 3 and Fig. 4). We also compare predicted and simulated drain conductance (Fig. 5). The model's predictions mostly agree well with simulations.

IV. Applying the Model to Circuit Design

We now use the developed device model to predict circuit behavior in the presence of mismatch and temperature variations. We analyze a current mirror, predict its output current, and verify against Spectre simulations.

A current mirror scales its input current, I_{in}, to generate an output current, $I_{\mathrm{out}} \equiv \mathcal{I}_{\mathrm{m}}(I_{\mathrm{in}})$. We studied an NMOS current mirror (N_1, N_2) feeding a PMOS diode-connected load (P_1) (Fig. 6). Assuming these three devices are in subthreshold saturation (i.e., $e^{-V_{\mathrm{DS}}/U_T} \ll 1$), their currents are given by

$$I_{\mathrm{in}} = \Lambda_{\mathrm{N1}} I_{\mathrm{off_N}} e^{\frac{\kappa_{\mathrm{N}} V_{\mathrm{GS_{N1}}}}{U_T}} e^{\lambda_{\mathrm{N}}\left(V_{\mathrm{GS_{N1}}} - V_{\mathrm{DS_{ref}}}\right)} \tag{20}$$

$$I_{\mathrm{out}} = \Lambda_{\mathrm{N2}} I_{\mathrm{off_N}} e^{\frac{\kappa_{\mathrm{N}} V_{\mathrm{GS_{N1}}}}{U_T}} e^{\lambda_{\mathrm{N}}\left(V_{\mathrm{DD}} + V_{\mathrm{GS_{P1}}} - V_{\mathrm{DS_{ref}}}\right)} \tag{21}$$

$$I_{\mathrm{out}} = \Lambda_{\mathrm{P1}} I_{\mathrm{off_P}} e^{-\frac{\kappa_{\mathrm{P}} V_{\mathrm{GS_{P1}}}}{U_T}} e^{\lambda_{\mathrm{P}}\left(-V_{\mathrm{GS_{P1}}} - V_{\mathrm{DS_{ref}}}\right)} \tag{22}$$

where $V_{\mathrm{GS_{N1}}}$ and $V_{\mathrm{GS_{P1}}}$ are N_1's and P_1's gate-source voltages, respectively, and I_{off} is given by

$$I_{\mathrm{off}} = I_{0_{\mathrm{nom}}} e^{\langle \gamma_1 \rangle \left(1 - \frac{T_{\mathrm{nom}}}{T}\right)} e^{\pm \frac{(1-\kappa) V_{\mathrm{BS}}}{U_T}}. \tag{23}$$

Λ_{N1}, Λ_{N2} and Λ_{P1} are independently and identically distributed (i.i.d) random variates defined in (14), with $\sigma_{1\text{-}2}$ set appropriately for NMOS and PMOS devices. Solving for I_{out} yields the current mirror's gain,

$$\frac{\mathcal{I}_{\mathrm{m}}^{\mathrm{N}}(I_{\mathrm{in}})}{I_{\mathrm{in}}} \cong \frac{\Lambda_{\mathrm{N2}}}{\Lambda_{\mathrm{N1}}} e^{\lambda_{\mathrm{N}} V_{\mathrm{DD}}} \left(\frac{\Lambda_{\mathrm{N2}} I_{\mathrm{off_N}}}{I_{\mathrm{in}}}\right)^{\frac{\lambda_{\mathrm{N}} U_T}{\kappa_{\mathrm{N}}}} \left(\frac{\Lambda_{\mathrm{P1}} I_{\mathrm{off_P}}}{I_{\mathrm{in}}}\right)^{\frac{\lambda_{\mathrm{N}} U_T}{\kappa_{\mathrm{P}}}}, \tag{24}$$

assuming that $\lambda U_T \ll \kappa < 1$. The gain deviates slightly from unity due to a dependence on I_{in} and T introduced by CLM. This prediction agrees well with the simulated current mirror gain (Fig. 6).

From the mismatch of these three devices, we now derive the distribution of the current mirror's gain. Due to transistor mismatch, it is drawn from $\mathrm{Lognormal}\,(\mu_{\mathrm{m}}, \sigma_{\mathrm{m}})$ with[1]

$$\mu_{\mathrm{m}} = \lambda_{\mathrm{N}} V_{\mathrm{DD}} + \lambda_{\mathrm{N}} U_T \log\left(\left(\frac{I_{\mathrm{off_N}}}{I_{\mathrm{in}}}\right)^{\frac{1}{\kappa_{\mathrm{N}}}} \left(\frac{I_{\mathrm{off_P}}}{I_{\mathrm{in}}}\right)^{\frac{1}{\kappa_{\mathrm{P}}}}\right), \tag{25}$$

$$\sigma_{\mathrm{m}}^2 = \left(\left(\left(1 + \frac{\lambda_{\mathrm{N}} U_T}{\kappa_{\mathrm{N}}}\right)^2 + 1\right)\sigma_{1_{\mathrm{N}}}^2 + \frac{\lambda_{\mathrm{N}}^2 U_T^2}{\kappa_{\mathrm{P}}^2}\sigma_{1_{\mathrm{P}}}^2\right)\frac{T_{\mathrm{nom}}^2}{T^2} + \left(\left(1 + \frac{\lambda_{\mathrm{N}} U_T}{\kappa_{\mathrm{N}}}\right)^2 + 1\right)\sigma_{2_{\mathrm{N}}}^2 + \frac{\lambda_{\mathrm{N}}^2 U_T^2}{\kappa_{\mathrm{P}}^2}\sigma_{2_{\mathrm{P}}}^2. \tag{26}$$

There is good agreement between output currents this distribution of gains predicts and Monte Carlo simulation results, across input currents and temperatures (Fig. 7). Deviations are mostly due to the channel-length modulation of N_1 and N_2, with negligible contribution from P_1.

V. Conclusion

We presented an analytical compact model for subthreshold MOS devices, with seven fitting parameters that capture mismatch and temperature variation. We only need to run an initial set of simulations on individual devices to extract parameter values, and then we can use the analytical model expressions to design circuits. The model also accounts for channel-length modulation and drain-induced barrier lowering. Both short and long channel devices are modeled, and a subthreshold current mirror design example is presented. Despite ignoring higher-order terms (see Eqs. 5 & 7), the developed model agrees with Spectre simulations in a reverse-body biased 28-nm FDSOI process in the commercial temperature range (error $< 10\%$ for $I_{DS} \geq 10$ fA across 0–50°C). Therefore, the analytical model saves the designer from having to run repeated, time-consuming Monte Carlo simulations on large circuits. To extend the model to a wider temperature range while maintaining accuracy, we may consider higher-order temperature dependence terms. The developed model is general and can be applied to the design of other subthreshold circuits, such as low-power silicon neurons. This model has guided the design of large systems of silicon neuron and synaptic filter circuits, such as Braindrop.

[1] $x \sim \mathrm{Lognormal}\,(\mu_{\mathrm{x}}, \sigma_{\mathrm{x}})$ and $y \sim \mathrm{Lognormal}\,(\mu_{\mathrm{y}}, \sigma_{\mathrm{y}}) \Rightarrow x^a y^b \sim \mathrm{Lognormal}\left(a\mu_{\mathrm{x}} + b\mu_{\mathrm{y}}, \sqrt{a^2\sigma_{\mathrm{x}}^2 + b^2\sigma_{\mathrm{y}}^2}\right)$

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