

### 6.3 Arbitrated Address Event Representation Digital Image Sensor

Eugenio Culurciello<sup>1</sup>, Ralph Etienne-Cummings<sup>1</sup>, Kwabena Boahen<sup>2</sup>

<sup>1</sup>Dept. of ECE, Johns Hopkins University, Baltimore, MD 21218

<sup>2</sup>Bioengineering Department, University of Pennsylvania, Philadelphia, PA 19104

An 80x60 (1/8 VGA) fully-arbitrated address event representation (AER) imager in a 0.6 $\mu$ m CMOS process converts light intensity into a one-bit code (a spike). The value of the intensity is inversely proportional to the inter-spike interval. The read-out of each spike is initiated by the pixel; each pixel requests access to the output bus, and its address (x, y locations) appears at the output after arbitration [1]. Therefore, the available output bandwidth is allocated according to a pixel demand. This read-out method favors brighter pixels, minimizes power consumption by remaining dormant until data is available and supports column-parallel read-out. In contrast, a serially-scanned array allocates equal portion of the bandwidth to all pixels independent of activity and continuously dissipates power because the scanner is always active. Representing intensity in the temporal domain allows each pixel to have a large dynamic range [2], [3]. The measured dynamic range for an individual pixel is 200dB (0.008Hz – 40MHz). Similarly, under uniform illumination, the array has a dynamic range of 120dB (40Hz – 40MHz). Figure 6.3.1 summarizes the characteristics of the array. The power consumption is 3.4mW in uniform indoor light (0.1mW/cm<sup>2</sup>) and produces a mean event rate of 200kHz (41.7 effective fps). Capable of 8.3k effective fps, this imager is one of the largest dynamic range [3], lowest power [4] and fastest [5] in the literature.

Operation of the imager is divided into three parts. First the light is integrated and converted into a 1b pixel request signal, next the row and column arbitration trees select which pixel to output and finally the pixel address is encoded and the pixel is acknowledged and reset.

Because of the output-on-demand nature of the imager, the integration, read-out and reset cycle is executed asynchronously. The read-out sequence queues and outputs spikes occur according to a Poisson process, because the pixels act independently. Consequently, the probability of an address from a certain region is proportional to the light intensity in that neighborhood. This is the first reported example of a probabilistic active pixel sensor (APS), where the output activity reflects the statistics of the scene. Figure 6.3.2 shows an example of the distribution of events for a typical lab scene.

The pixel is modeled after an APS, but also includes additional asynchronous address-event circuitry. Figure 6.3.3 shows the schematic of the pixel. Photons collected by an n-type photodiode are integrated on a 0.1pF capacitor, to give a slew-rate of 0.1V/ms in typical indoor light (0.1mW/cm<sup>2</sup>). Because the slew-rate can be in low light, the comparator for generating the pixel request signal must have a fast switch time with low power consumption. Using an inverter with positive feedback (Figure 6.3.4), results in 3ns switch time using only 0.084pJ (simulated). A typical inverter of similar size and speed uses about 0.18pJ. The majority of the pixel power consumption occurs during reset. To reduce reset power, the integration capacitor is disconnected from the comparator when a request is generated. The capacitor is then reset from  $-(V_{dd} - V_{tp})$  to  $V_{dd}$  instead of Gnd to  $V_{dd}$ . During reset, 3.88pJ (simulated) is used. The array, including the comparator, dissipates 100 $\mu$ W at  $V_{dd\_analog} = 2.75V$  running at 200kHz in uniform room light ( $\sim 0.1mW/cm^2$ ). When

imaging a typical indoor scene, the analog power consumption drops to below 10 $\mu$ W.

The circuits for generating the pixel request and receiving an acknowledge/reset are also shown in Figure 6.3.3. When the comparator is triggered, a row request,  $-p$ , is generated. The row arbitrator picks one active row. The selected row is copied into a buffer sitting above the array. The signal  $li$  indicates which pixel in the row has issued a request. This buffer provides a pixel access speed-up and improved parallelism by realizing a pipelined read-out scheme. Once copied, the entire row is acknowledged/reset (signal  $s$ ), the row address is generated by a ROM, and photon integration starts anew. Column arbitration is performed on the buffered row. The arbitration tree selects the active elements in the buffer, computes and outputs their addresses before clearing the buffer. A new active row is obtained when the buffer is clear. Performing column arbitration on the buffered row also improves read-out speed by eliminating the large capacitance associated with the column lines that is encountered when arbitration is done within the array. Figure 6.3.4 shows the architecture of the row and column arbitration circuits.

The entire imager, analog and digital parts, consumes 3.4mW at  $V_{dd\_digital} = 2.9V$  in 0.1mW/cm<sup>2</sup> light (0.2MHz). The relationship between event (output) frequency and power consumption is given by  $P[mW] \approx 1.7F[MHz] + 3.1$  (empirical curve fit), where  $F$  is the event frequency. The static dissipation is produced by the pseudo-CMOS logic used in this design. At full speed (40MHz), and maximum array dynamic range (6 decades), the power consumption is 71mW. Normal operation produces events at a maximum of 4MHz, for a dynamic range of 5 decades, while consuming 10mW. A full VGA with 3 decades of dynamic range operates at 2.46MHz and consumes only 7.3mW. Figure 6.3.5 shows how the output rate per pixel, dynamic range, power and array size scale.

Imaging with this chip requires a specialized digital frame grabber, composed of a high-resolution timer ( $\sim 24b$ ) and a large frame buffer ( $\sim 15MB$  for VGA). The timer indexes each event and compares it with the last time an event at that pixel was recorded. The difference is inversely proportional to the light intensity. The buffer must hold the latest pixel time index and the intensity value. Figure 6.3.6 shows example images recorded with the array. Note that features in the shadows can be seen using a log plot.

#### Acknowledgements:

This work was supported by an NSF CAREER award to Dr. Etienne-Cummings and a Whitaker Foundation award to Dr. Boahen. Special thanks to A. Andreou, P. Pouliquen, C. Wilson and A. van Schaik for insights.

#### References:

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Technology	0.6µm 1M2P CMOS
Array Size	80 (H) x 60V
Pixel Size	32µm x 30µm
Fill Factor	34%
Dynamic Range	30dB (Pix.) 120dB (Array)
Bandwidth	80Hz - 40MHz (Pix.) 40Hz - 40MHz (Array)
Pixel Frequency Jitter (STD/Max)	6x10 <sup>-5</sup> %
Sensitivity (Hz/mW/cm <sup>2</sup> )	2x10 <sup>6</sup> (Array) 42 (Pix.)
FPN (STD/Mean) @ 0.1 mW/cm <sup>2</sup>	4%
Max. FPS	8.3K (effective)
Digital Power @ 2.9V Supply	11.7fJ/bit/13.1mW 3.4µW @ 0.1mW/cm <sup>2</sup>
Analog Power @ 2.7V Supply	< 10µW for scene @ 0.1mW/cm <sup>2</sup>

Figure 6.3.1: Summary of chip characteristics.

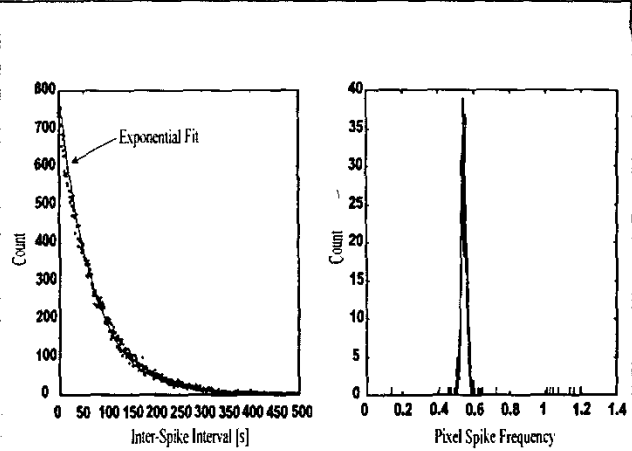


Figure 6.3.2: Poisson distribution of events. Inter-spike interval (left) and variation (right).

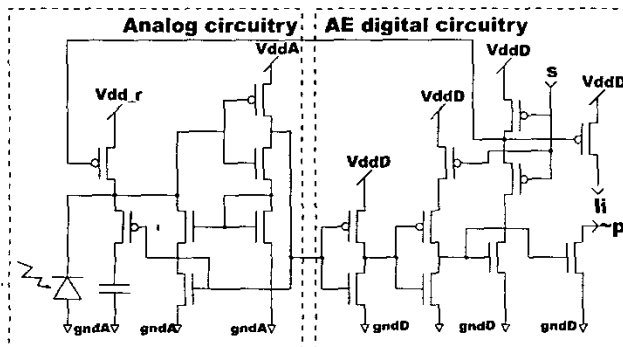


Figure 6.3.3: Pixel schematic.

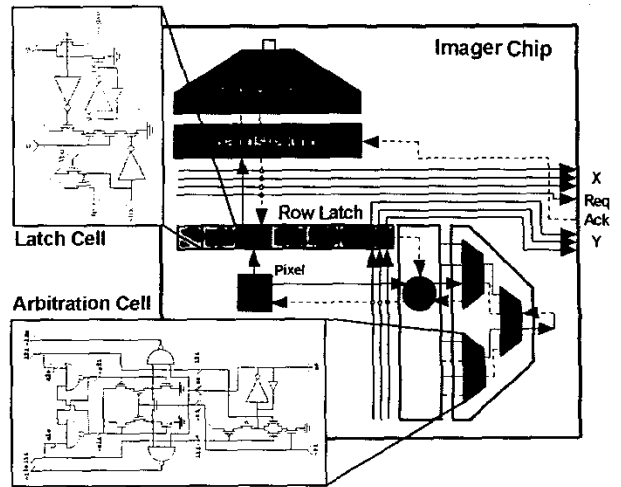


Figure 6.3.4: Row and column arbitration architecture.

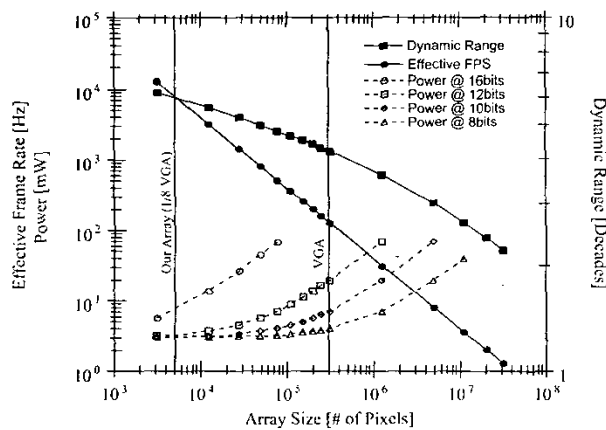


Figure 6.3.5: Scaling properties of the array. Power is computed for a fixed dynamic range.



Figure 6.3.6: Example images. Linear intensity (left) and logarithmic (right) scales.