Signature: _____ Last name (print): _____

EE486—Advanced C[illegible]rithmetic
Professor M. Flynn

Midterm Exam

1. For RN and RP, show the final rounded results in the following cases:

s	Exponent	Fraction	Guard	*S*
0	00011111	11111111111111111111111	1	0
0	11111110	11111111111111111111111	1	1
1	11111110	11111111111111111111111	1	1
0	00000000	11111111111111111111111	1	0

	s	Exponent	Fraction	Comment
RN				

	s	Exponent	Fraction	Comment
RP				

2. In recent years, there have been a number of Stanford theses (Santoro, Song, Bewick) showing the advantages of various counter configurations.

   (a) Show a (7,3) and a "(4,2)" counter made from GSA's—i.e., (3,2) counters.

   (b) For an IEEE multiply using 2-bit Booth, assume we require partial product height 28 (54/2 + 1).

   For the middle bits (h = 28), show the reduction of the partial produce tree to two inputs to a CPA. Using counters

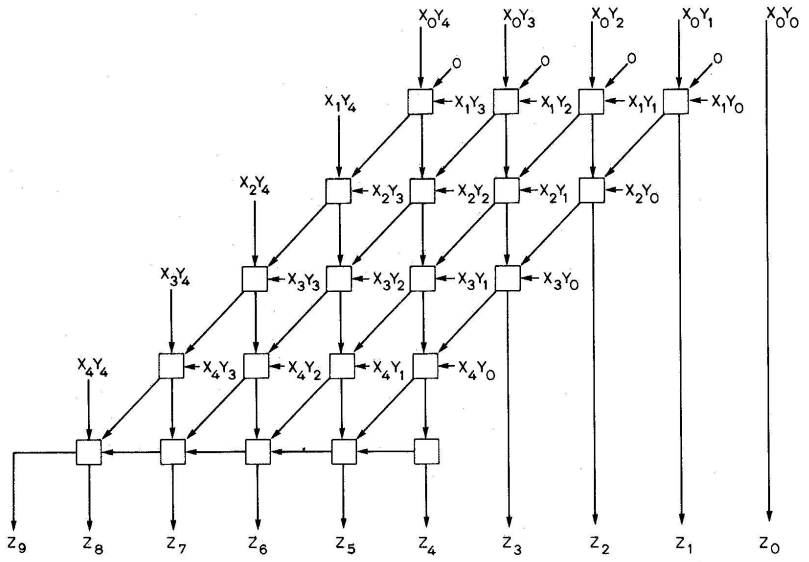
   (a) (7,3) —reduce to 3 and use a single CSA to input to the CPA

   (b) "(4,2)"

   (c) (3,2)

   Approximately how many counters are required for each, and how many serial CSA delays before entry to the CPA?

3. In an effort to simplify multiplication layout and control, linear arrays of adder cells have been suggested [Pezaris, 1971]. Here, each cell is a full adder that adds a pp bit $x_i y_j$ with the sum output from $x_{i-1} y_{j+1}$ and carry from x_{i-1}, y_{j-1}.



Each adder has a delay of 2 units. For this array approach, the delay to form a product of 48×48 operands is _____. The approach uses _____ adder cells.

A Wallace tree would use _____ levels of CSA and have an overall delay of _____ (for CPA, assume $r = 3$, CLA implementation). Show computation. Approximately how many CSA are required in the Wallace approach? _____.

Can the linear array be used with Booth? Explain.

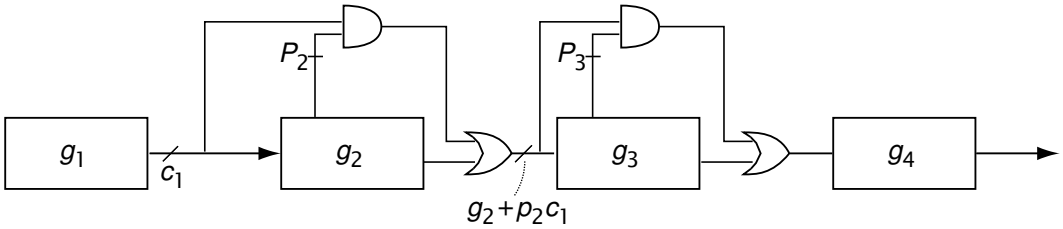
4. A $55^b \times 55^b$ (unsigned operands) multiplier is to be implemented using 2^b modified Booth to generate the partial products and one level of (7,3) counters to iterate on the partial products before entry into a CPA. Using λ as a unit delay, assume it takes 5λ for pp generation, 5λ for (7,3) counter iteration, and 10λ for a CPA. The pp tree height is _____. If each iteration retries the same number of (encoded) pp's, _____ iterations are required.

   Each iteration resolves (i.e., completes processing) on _____ bits of the product. A total of _____ bits (the dot count) of pp are fed back to the (7,3) counters for each iteration. At the end of the last iteration, the results must be assimilated by a CPA. Show timing and explain.

   What is required to do this other than a 110^b CPA? _____.

   A small improvement is possible in the final CPA by pipelining the entry into the CPA. This provides the least significant bits of the product early. The final CPA must now be _____ bits. Show new timing and explain.

5. Carry skip adders are a type of inexpensive adder where a ripple carry within a group is combined with a simple group bypass, based on a group propagate signal. So we have:



Suppose it takes 2 units of delay to form a bit sum or bit carry. Each AND and OR gate has one unit delay. It would take 32 delay units for a 16-bit adder to generate either the worst sum or carry. **Note:** the worst case may be any of the sum bits as well as the carry.

(a) In a 16-bit adder with 4 groups of 4 bits each, the (worst case) delay is _____. Show this path.

(b) Suppose we now allow variable bit size groupings. If we retain the structure drawn above (each group must have at least one bit), what is the optimum bit grouping?

g_1 _____ g_2 _____ g_3 _____ g_4 _____

This gives _____ delay (worst case).

(c) Now suppose we vary the allowable number of groups, but the structure must still follow the figure. Find a better delay than above. For your solution:

What is the number of groups? _____.

What is the assignment of bit sizes to each group? _____.

What is the resultant (worst case) delay? _____.