Lecture #13: Random Topics

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Administrivia

- Has everyone demoed Lab 6 lab?
  - If not, it's due at end of lab Thursday evening.
- Project Milestone #1 is due Thursday Feb 28th at 10pm.
- Midterm #2 is in class Thursday Feb 28th.
- Paul's near-term office hours:
  - Tues from 12:30-2:30pm
  - Wed from 10am-noon

Midterm Topics

- Lectures 8-12
- State Machine Design
- FSM Timing (max path/min path)
- Latches, Flops, & Metastability
- Memory architectures (ROM, SRAM, DRAM, etc)
- Focus will be on material in lecture.
  - Readings as specified in notes.

State Machine Design Process

1. Determination of inputs and outputs.
2. Determination of machine states.
3. Create State/Bubble Diagram—should this be a Mealy or Moore machine?
4. State Assignment—assign each state a particular value.
5. Create Transition/Output Table
6. Derive Next State Logic for each state element—using K-maps as necessary.
7. Derive Output logic.
8. Implement in Xilinx.

More Detail of Provided VGA code from Lab 5

- Two parts
- VGA_SYNC
  - It gives you a X,Y and you give it a color to display.
- Instead of drawing directly use TCGROM
  - Text Character Generation Rom
  - Can be used to create any pattern → Sprites
  - Why are low order bits of X,Y not used?
- Watch timing!!! It must meet 25MHz.
  - Strategies if you don't?

RAM/ROM in Xilinx

- Distributed RAM initialization works fine.
  - Use CoreGen to create initialization file
- Block RAM only works with back annotated design file.
  - As far as we can tell, this is a bug.