Lecture #12: The Memories…, ahh the Memories…

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Administrivia

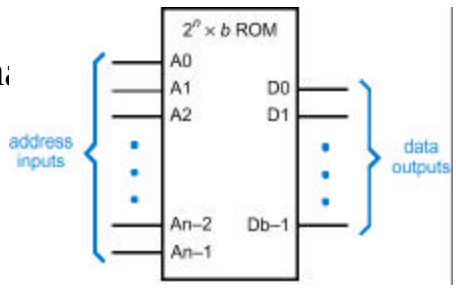
- Make sure to fill out TA evaluations!!!
  - Incentive: 5 Point bonus on Lab 6
    - Lab 6 is only worth 60
  - Everything is anonymous
- Lab 6 Prelab is due Midnight on Thursday.
  - This allows Thursday section to have a lab section to work on the hardware.
- Reading:
  - 10.1-10.4
- Project is Assigned Today

Memories in Digital Design

- Special Idiom in logic design.
- Different types of lookup tables (LUTs)
  - Same basic idea we have seen in the FPGA architecture.

Read-Only Memory (ROM)

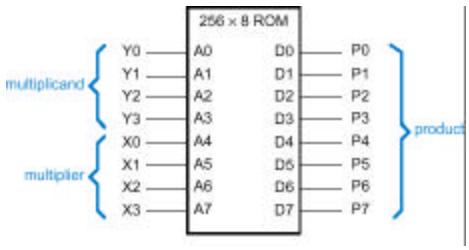
- Provide address and get data out
- Useful to implement complex random logic
  - Ie, Multi-bit XOR
- Really combinationa



Multiplier in ROM

Table 10-3 Hexadecimal text file specifying the contents of a 4 × 4 multiplier ROM.

```
00: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
10: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D
20: 00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A
30: 00 03 06 09 0C 0F 12 15 18 1B 1E 21 24 27
40: 00 04 08 0C 10 14 18 1C 20 24 28 2C 30 34
50: 00 05 0A 0F 14 19 1E 23 28 2D 32 37 3C 41
60: 00 06 0C 12 18 1E 24 2A 30 36 3C 42 48 4E
70: 00 07 0E 15 1C 23 2A 31 38 3F 46 4D 54 5B
80: 00 08 10 18 20 28 30 38 40 48 50 58 60 68
90: 00 09 12 1B 24 2D 36 3F 48 51 5A 63 6C 75
A0: 00 0A 14 1E 28 32 3C 46 50 5A 64 6E 78 82
B0: 00 0B 16 21 2C 37 42 4D 58 63 6E 79 84 8F
C0: 00 0C 18 24 30 3C 48 54 60 6C 78 84 90 9C
D0: 00 0D 1A 27 34 41 4E 5B 68 75 82 8F 9C A9
E0: 00 0E 1C 2A 38 46 54 62 70 7E 8C 9A A8 B6
F0: 00 0F 1E 2D 3C 4B 5A 69 78 87 96 A5 B4 C3
```

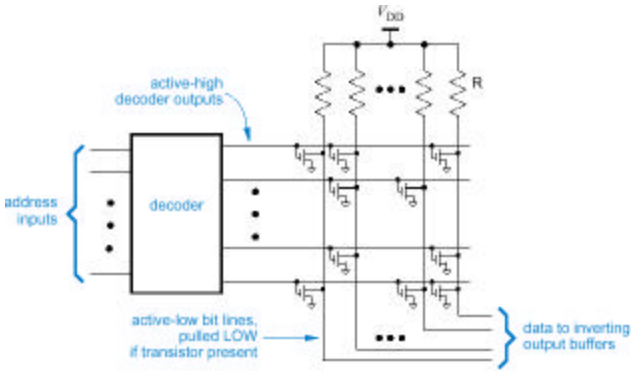


Pentium Bug—Whoops!!

- The infamous Pentium bug was caused by a ROM that was misprogrammed:
  - "The fault itself had occurred because of the omission of five entries in a table of 1,066 values (part of the chip's circuitry) used by a speedy algorithm…The five cells should have contained the constant +2, but because the cells were empty, the processor fetched a zero."
  - http://www.maa.org/mathland/mathland_5_12.html

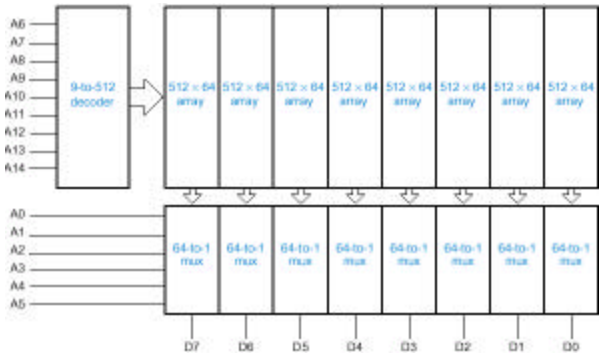
ROM Internal Structure

- Transistor in place indicates 1 (or vice versa depending on output polarity)



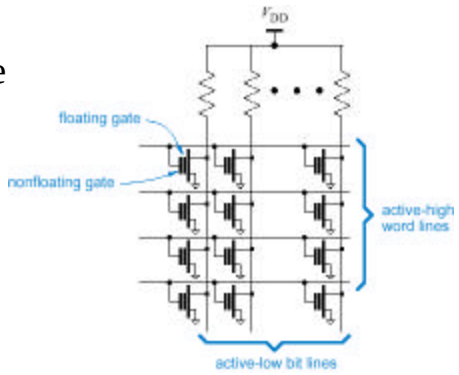
Two-Dimensional Decoding

- Split address into row and column addressing…



ROM state elements

- There are many techniques used to configure a ROM state element
  - Blow a fuse or "refill" a floating gate

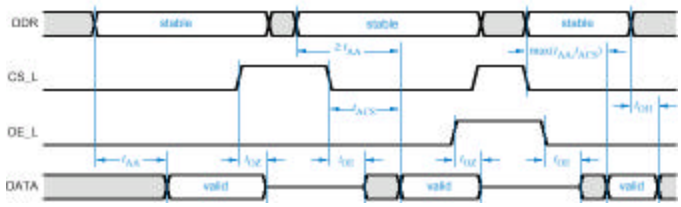


FLASH "RAM"

- Must reprogram entire sector—not random access programmable.
- Only reprogrammable a limited number of times
- The XSA-100 board has a flash on it
  - Reprogram to all 0's and write appropriate 1's
  - Typical 10,000 Write Cycles
- http://www.atmel.com/atmel/acrobat/doc1008.pdf

ROM Timing

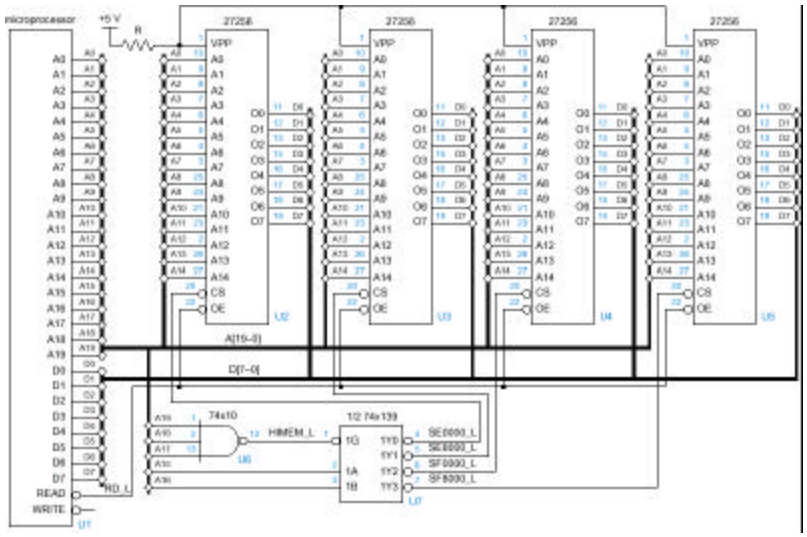
- Kind of what you might expect.
  - Chip Select and Output Enable



Use Output Enables to Gang Parts

- Multiple parts of any memory type can be combined to make a larger system using the tristate outputs of the data bus.

Ganging…

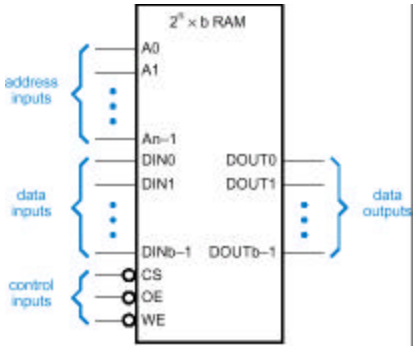


RAM

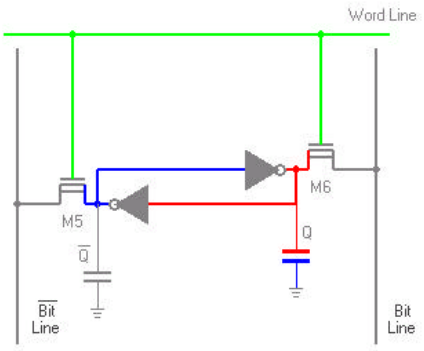
- Static RAM (SRAM) requires no refresh cycles
  - Faster, more expensive, less dense
- Dynamic RAM (DRAM) requires a refresh cycle to keep the values current in the memory
  - Slower, less expensive, more dense

SRAM

- Can now write data so need data input signals.
- Need way to indicate that a write should be performed
  - Write Enable signal



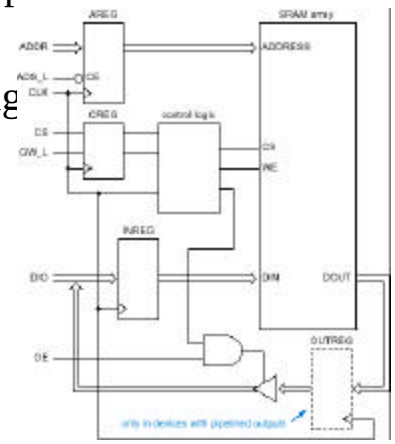
SRAM 6T cell



- http://jas2.eng.buffalo.edu/applets/education/system/memcells/sramcell/index.html

Synchronous SRAM (SSRAM)

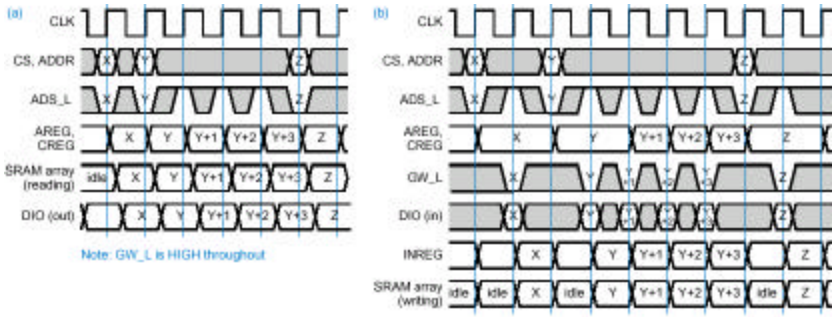
- When flop-ed at the output called "registered"
- Helps meet board timing



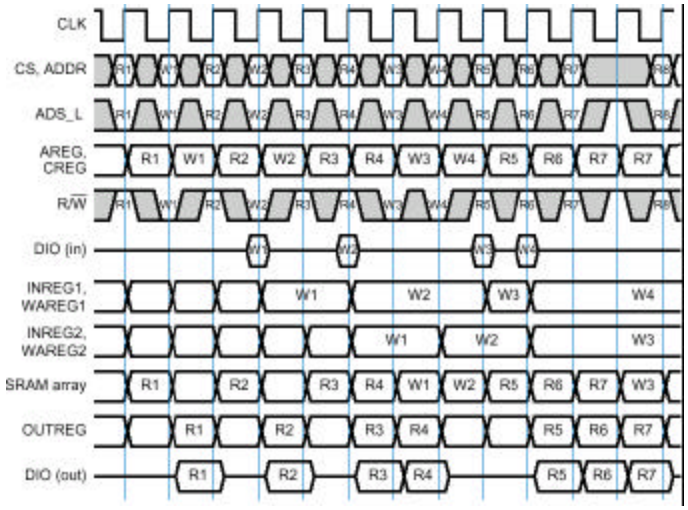
Bus Interfaces to RAM

- The turn-around penalty is involves alternating from reading to writing (& vv)
  - Requires three cycles for back-to-back read and writes.
- Delay write by providing data on next cycle.
  - Zero-Bus Turnaround (ZBT) architecture

Regular SRAM timing



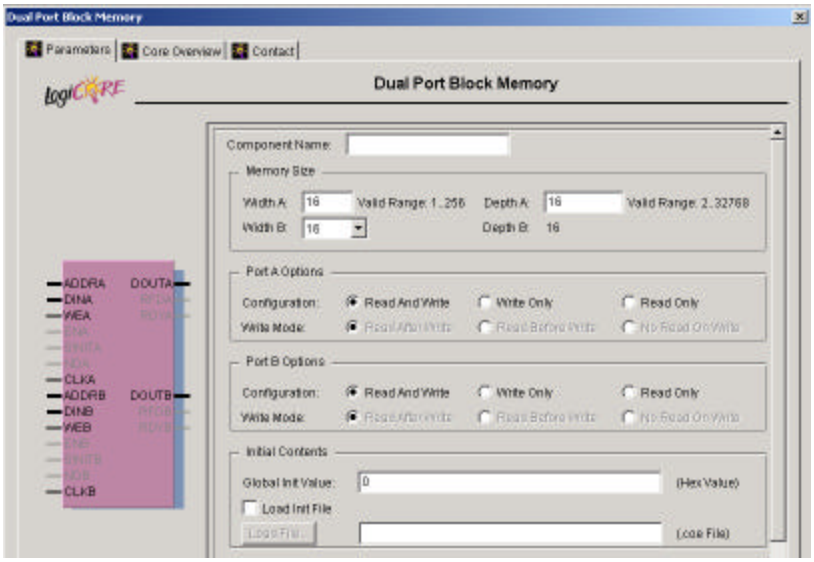
ZBT Timing Diagram



Two Port & Dual Port

- What if you had two ports for reading and writing and accessed the same location.
  - What happens? Depends on the device
  - Old data, new data, bad data…
- If you have separate clocks then basis of circuit to pass data between clock domains…

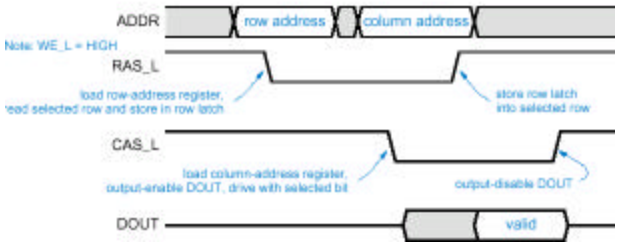
Xilinx Dual Port Block RAM



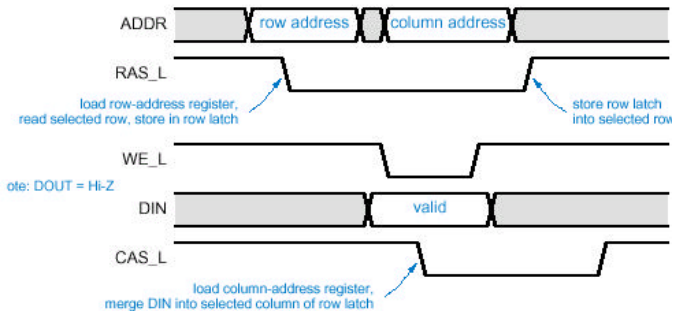
Dynamic RAM

- SRAM like structure but present the row and column addresses separately and sense amplifier on bit lines detects output data.
- Can be Synchronous and have registered outputs.
- The one on the XSA-100 board is http://www.hynix.co.kr/datasheet/pdf/dram/(2)HY57V281620A(L)T-I.PDF

DRAM Read Timing

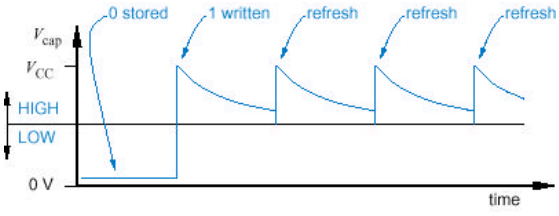


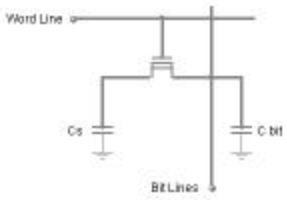
DRAM Write Timing



DRAM is based on 1T cell

- Needs Refreshing every 64ms





- http://jas2.eng.buffalo.edu/applets/education/system/memcells/dramcell/index.html

DRAM Refresh Timing

A better DRAM cell

- "Toshiba cuts capacitor from DRAM cell design"
  - Toshiba Corp. has developed a one-transistor, no-capacitor cell structure that it claims solves the difficulties encountered in producing DRAMs in sub-0.1-micron process technology.
  - http://www.eetimes.com/story/OEG20020207S0064