Lecture #11: Latches, Flops, and Metastability

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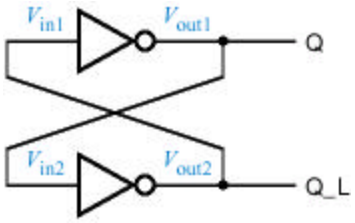
Administrivia

- Make sure to fill out TA evaluations!!!
  - Incentive: 5 Point bonus on Lab 6
    - Lab 6 is only worth 60
  - Everything is anonymous
- Lab 6 Prelab is due Midnight on Thursday.
  - This allows Thursday section to have a lab section to work on the hardware.
- Reading:
  - 7.1, 7.2.1, 7.2.3-7.2.7
  - 8.8-8.9 (only skim 8.9.8)

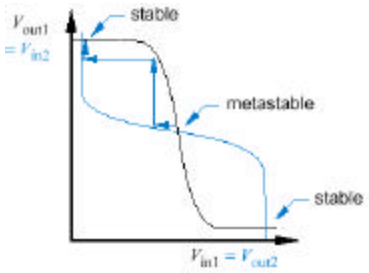
Bistable Element

- What are the stable operating regimes of this device?
  - Either Vout1 or Vout2 is high, right?

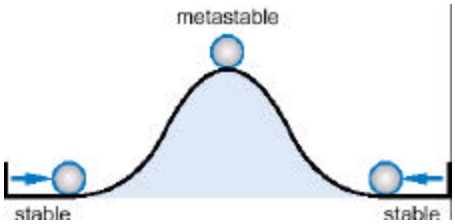


Analog Analysis

- There are two stable points but one "metastable" point.
  - Will leave metastability eventually because of random fluctuations.

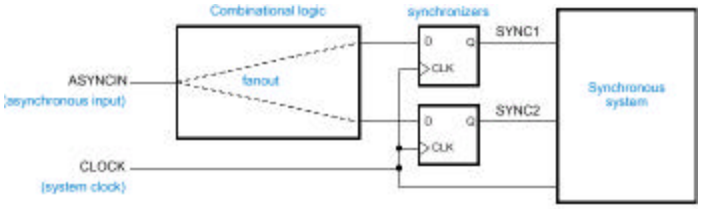


Physical Analogy



Fanout causes problems

- Each flop may interpret the signal differently if it is metastable.
  - Big Problem…



How to Avoid?

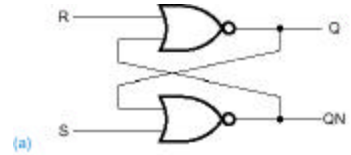
- If the *simplest* sequential circuit is susceptible to metastable behavior, you can be sure that *all* sequential circuits are susceptible.
  - And this behavior is not something that only occurs at power-up.
- This is a fundamental issue.
  - All you can do is wait…
  - Just like waiting for a stick on end to fall.

Latches and Flip-Flops

- A **flip-flop** samples its inputs and changes its inputs only at times determined by a clocking signal.
- A **latch** watches all of its inputs continuously and changes its outputs at any time, independent of a clocking signal.

SR Latch

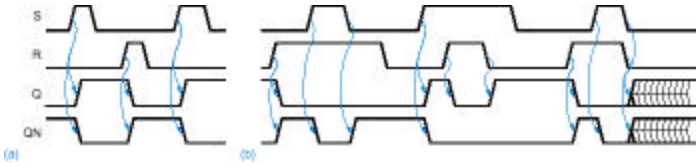
- Same as in E40…



S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

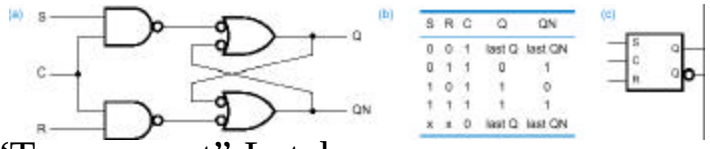
(b)

- There are invalid states…



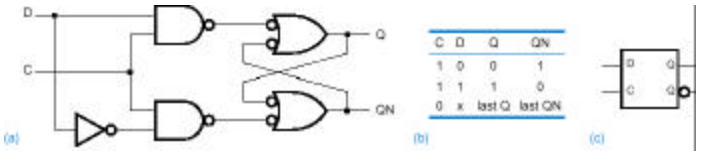
Clumsy so add Enable and D

- Called clock but not really…



S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	last Q	last QN

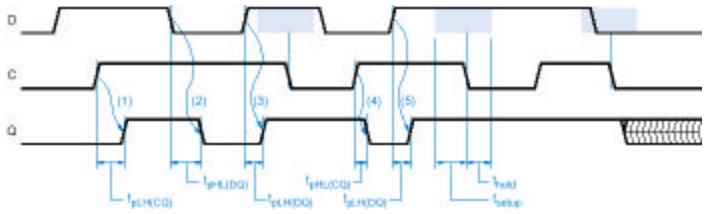
- "Transparent" Latch



C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

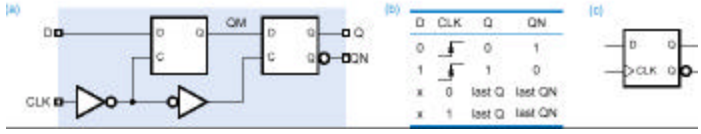
D Latch Timing

- Note propagation delay, setup and hold times

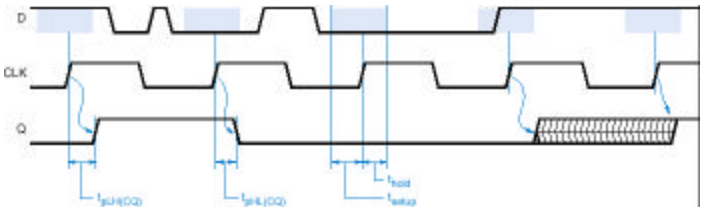


Use Two Latch to Make Edge-Triggered Device

- Master-Slave Design

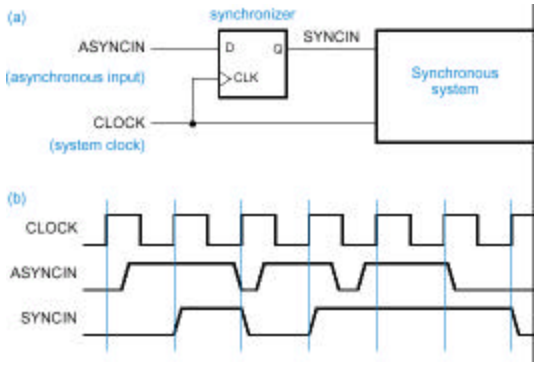


- Still have metastability issue



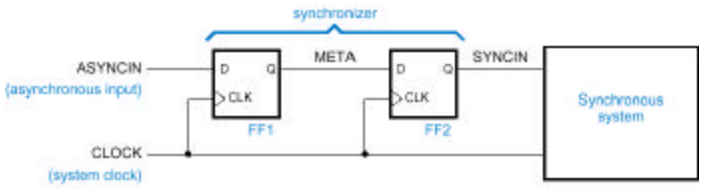
Asynchronous Inputs

- Have to convert “real-world” inputs for use in synchronous system.



More Time!

- Give the signal more time to settle out.
  - Does not solve the problem!!
- This is the recommended design.



MTBF Formula

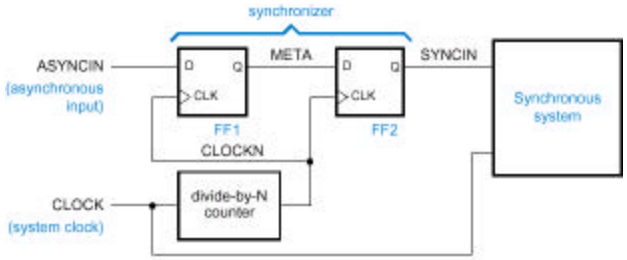
- Mean Time Between Failures
- If the synchronizer waits time tr, what is the time on average before failure occurs.
  - MTBF(tr) = exp(tr/tau) / To * f * a
- Make this value “large”

Metastability Param Values

Table 8-35 Metastability parameters for some common devices.

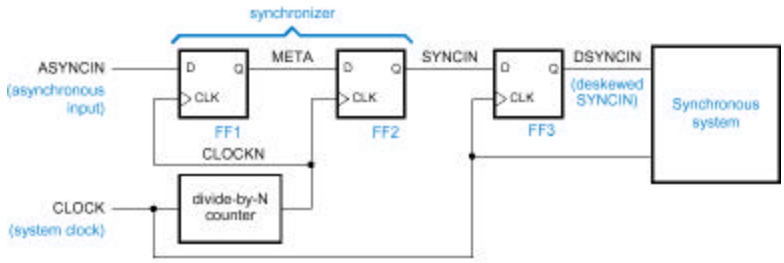
Reference	Device	τ (ns)	T_o (s)	t_r (ns)
Chaney (1983)	74LS74	1.50	$4.0 \cdot 10^{-1}$	77.71
Chaney (1983)	74S74	1.70	$1.0 \cdot 10^{-6}$	66.14
Chaney (1983)	74S174	1.20	$5.0 \cdot 10^{-6}$	48.62
Chaney (1983)	74S374	0.91	$4.0 \cdot 10^{-4}$	40.86
Chaney (1983)	74F74	0.40	$2.0 \cdot 10^{-4}$	17.68
TI (1997)	74LSxx	1.35	$4.8 \cdot 10^{-5}$	63.97
TI (1997)	74Sxx	2.80	$1.3 \cdot 10^{-9}$	90.33
TI (1997)	74ALSxx	1.00	$8.7 \cdot 10^{-6}$	41.07
TI (1997)	74ASxx	0.25	$1.4 \cdot 10^{3}$	14.99
TI (1997)	74Fxx	0.11	$1.9 \cdot 10^{8}$	7.90
TI (1997)	74HCxx	1.82	$1.5 \cdot 10^{-6}$	71.55
Cypress (1997)	PALC16R8-25	0.52	$9.5 \cdot 10^{-12}$	14.22*
Cypress (1997)	PALC22V10B-20	0.26	$5.6 \cdot 10^{-11}$	7.57*
Cypress (1997)	PALCE22V10-7	0.19	$1.3 \cdot 10^{-13}$	4.38*
Xilinx (1997)	7300-series CPLD	0.29	$1.0 \cdot 10^{-15}$	5.27*
Xilinx (1997)	9500-series CPLD	0.17	$9.6 \cdot 10^{-18}$	2.30*

Got More Time?



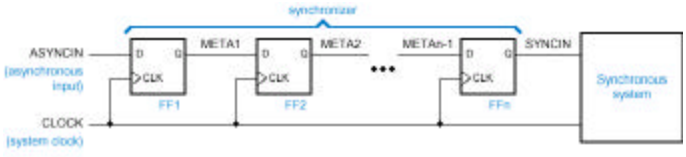
Nope…

- Don’t gate the clock!!!!!



Add more stages…

- Based on MTBF calculation



How many stages needed?

- See Xilinx App Note on Metastable Recovery
  - http://support.xilinx.com/xapp/xapp094.pdf
- Current FlipFlops have very high gain which helps pull out of metastability
  - Does not **solve** it…
  - Is a million years enough?
  - Remember Y2K!! ☺

Watch your edge detectors…