Lecture #10: FSM Timing

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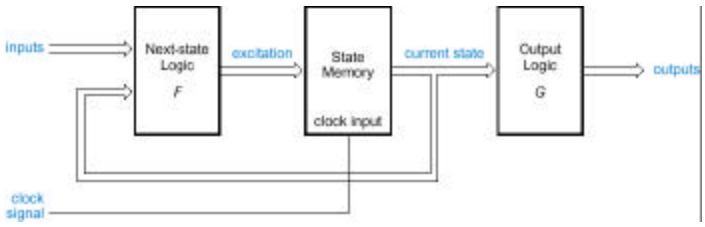
FSM Timing

- Now that we now how to design a state machine, how fast can we make it run?
- The register-to-register performance is the key metric to consider.

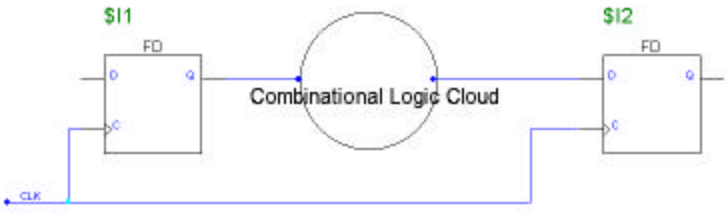


Clock Skew

- We have assumed that the clock reaches each DFF simultaneously.
  - It should be no surprise that this assumption is not entirely valid.
- Clock Skew is the non-time varying (static) difference in the clock arrival time at two different DFFs.

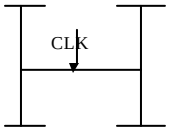
Clock Skew II

- The wire propagation delay is non trivial and the difference in arrival times for this type of layout is unacceptable.



H Clock Distribution Tree

- Make Clock distribution tree in the form of an H so that all flops are equidistant to the root of the tree.
- An FPGA is a very regular structure but for an ASIC, there are a variable number of DFFs in each sector.



Spartan II Skew Data

XILINX®

Spartan-II 2.5V FPGA Family: DC and Switching Characteristics

Clock Distribution Guidelines(1)

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
GCLK Clock Skew				
$T_{GSKEWIOB}$	Global clock skew between IOB flip-flops	0.13	0.14	ns

Notes:
1. These clock distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Jitter

- Clock Jitter is the time-varying (cycle to cycle) difference in the clock arrival time at the ***same*** DFF.
- There are many sources of jitter—inaccuracies in the source oscillator, drifting of the Phase Lock Loop (PLL), and crosstalk between the clock and other transitioning signals.

Spartan II Jitter Data

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 1, page 13, provides definitions for various parameters in the table below.

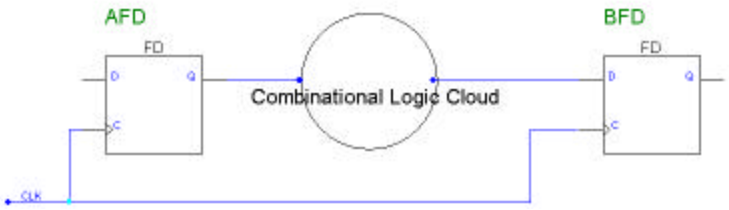
Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{LJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OUTCC}	Output jitter (cycle-to-cycle) for any DLL clock output[1]		-	±60	-	±60	ps
T_{PHO}	Phase offset between CLKIN and CLKO[2]		-	±100	-	±100	ps
T_{PHDO}	Phase offset between clock outputs on the DLL[3]		-	±140	-	±140	ps
T_{PHOM}	Maximum phase difference between CLKIN and CLKO[4]		-	±160	-	±160	ps
T_{PHDOM}	Maximum phase difference between clock outputs on the DLL[5]		-	±200	-	±200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, excluding input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, excluding output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, excluding Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (excluding input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output Jitter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (excluding input clock jitter).

Example Parameters

- DFF values:
  - $T_{clk->q}$=1ns, T_{setup}=1ns, T_{hold}=1ns
- Clock skew is max 2ns and jitter is 2ns
- Combinational logic T_{cl_pdmax}=10ns, T_{cl_pdmin}=1ns



MaxPath Timing Constraint

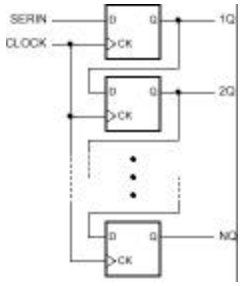
- Add up the components that result in the time budget; the period must be greater than this value.
- $T_{clk->q}+T_{cl\_pdmax}+T_{setup}+T_{skew}$ <= Clock Period
- 1 + 10 + 1 + 2 <= Clock Period
- 14ns <= Clock Period
- Max Frequency is 71MHz

MinPath Timing Constraint

- Consider what happens when the same clock edge is considered at the far DFF.
- $T_{clk->q} + T_{cl\_pdmin} >= T_{skew} + T_{hold}$
- 1 + 1 >= 2 + 1
- Whoops!! ☹
- AKA, “Hold-Time Violation”

MinPath and ShiftRegisters

- Shift Registers can easily fall prey to min path timing violations.
- Fix the violations by increasing delay between Ds and Qs
  - Insert pairs of inverters
- FPGA DFF clk->q is big enough so that MinPath violations are rare.



Impacts

- You can “fix” MaxPath timing constraint violations by slowing down the clock after the circuit is implemented.
- You ***cannot*** “fix” MinPath timing constraint violations be modifying the clock.

Static Timing Tool

- Longest MaxPath Constraint is called ***Critical Path*** of design.
  - Find critical path by calculating all the MaxPath constraints of ever every path in the design and picking the largest.
- Perfect tool for a computer.
  - Xilinx Timing Analyzer is an example of a static timing tool.

Timing Closure Challenges

- When integrate individual blocks that meet timing, the combined system might not meet timing.
- In general have registered outputs from ***top-level*** blocks.
  - This doesn't solve the problem if the chip is so large/fast that a signal cannot propagate all the way across the chip.
  - Reason that I/Os are always useful to register
    - Not always certain timing budget available on the board.

Lab 6 Discussion

- Lab 6 Objectives are to use the CODEC and SDRAM interfaces to build a simple music player.
  - And do another state machine of course… ☺