Lecture #9: Sequential Logic Idioms

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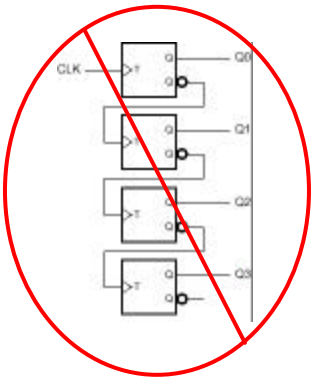
State Machine Design Process

1. Determination of inputs and outputs.
2. Determination of machine states.
3. Create State/Bubble Diagram—should this be a Mealy or Moore machine?
4. State Assignment—assign each state a particular value.
5. Create Transition/Output Table
6. Derive Next State Logic for each state element—using K-maps as necessary.
7. Derive Output logic.
8. Implement in Xilinx.

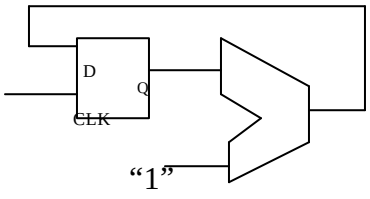
Counters (DDPP 8.4)

- Ripple Counters gate the clock and so are ***not*** acceptable



Synchronous Counter

- Counting is simply adding “1” to previous value.
- Use CoreGen to create Counters

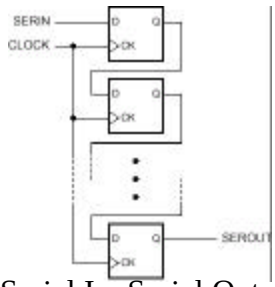


Modulo-n Counter

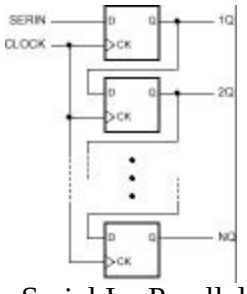
- If only the MSB of the Counter is considered, the counter creates a pulse every n seconds.
  - Used to create a slower periodic signal than core system clock.
  - Feed into synchronous enables to make state machines run slower
    - See Lab 5 Skeleton example.

Shift Registers (DDPP 8.5)

- Used to Convert from serial data stream to parallel data stream and vice versa

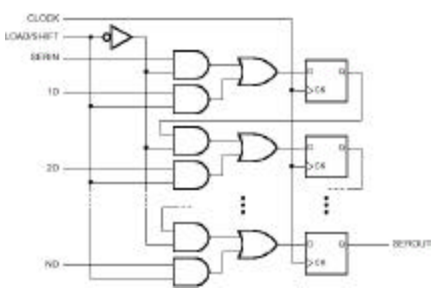


Serial-In, Serial-Out

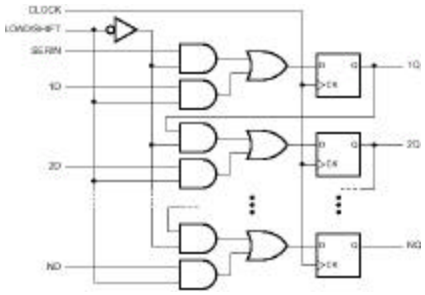


Serial-In, Parallel-Out

More Shift Registers



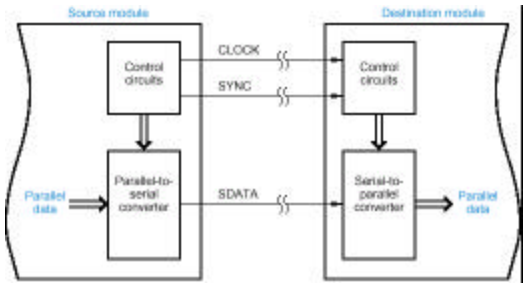
Parallel-In, Serial-Out



Parallel-In, Parallel-Out

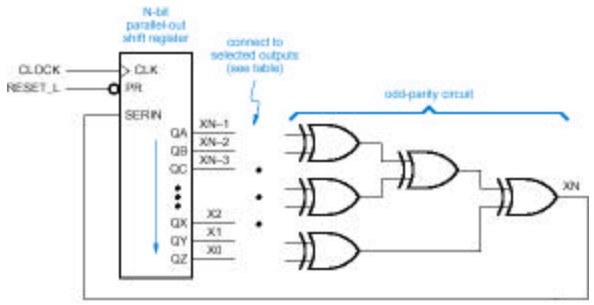
Shift Register Applications

- Reduce Number of wires between components in a system
  - If high speed, call SerDes (Serializer, Deserializers)
  - Must make sure to synchronize signals….



LFSR (DDPP 8.5.8)

- Linear Feedback Shift Register
  - Non Binary Counter
  - Counts 2^n –1 states



LFSR Feedback Logic

n	Feedback Equation
2	X2 = X1 ⊕ X0
3	X3 = X1 ⊕ X0
4	X4 = X1 ⊕ X0
5	X5 = X2 ⊕ X0
6	X6 = X1 ⊕ X0
7	X7 = X3 ⊕ X0
8	X8 = X4 ⊕ X3 ⊕ X2 ⊕ X0
12	X12 = X6 ⊕ X4 ⊕ X1 ⊕ X0
16	X16 = X5 ⊕ X4 ⊕ X3 ⊕ X0
20	X20 = X3 ⊕ X0
24	X24 = X7 ⊕ X2 ⊕ X1 ⊕ X0
28	X28 = X3 ⊕ X0
32	X32 = X22 ⊕ X2 ⊕ X1 ⊕ X0

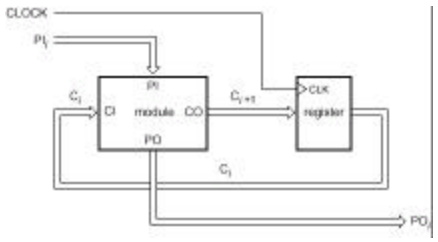
Table 8-21 Feedback equations for linear feedback shift-register counters.

LFSR Applications

- LFSR's used to create pseudo-random bit sequences.
- Also, very small and compact synchronous counter.
  - Very fast
  - Why faster than binary?

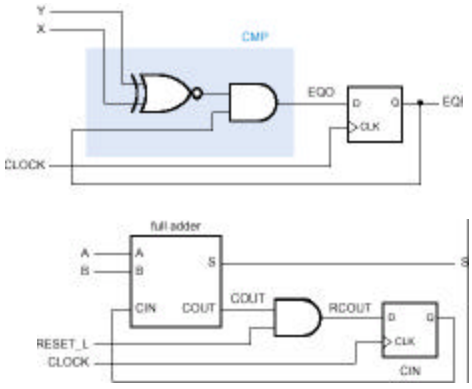
Iterative vs Sequential Circuits

- DDPP 8.6
- Space vs Time Tradeoff



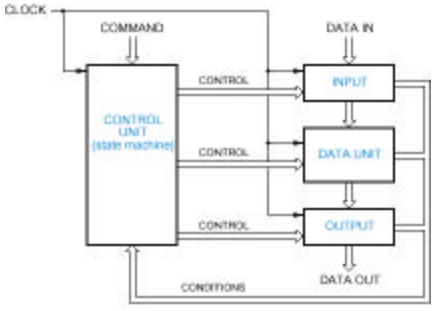
Serial Synchronous Circuits

- Small but long latency



Another view of Decomposition

- DDPP 8.7



VGA Circuit

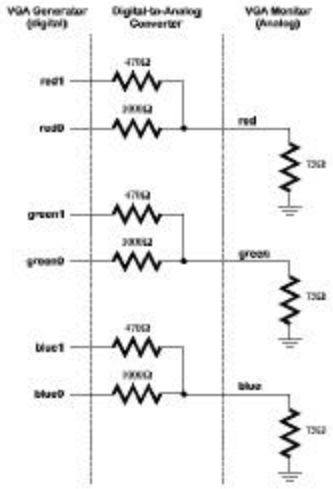


Figure 1: Digital-to-analog VGA monitor interface.

VGA Waveform

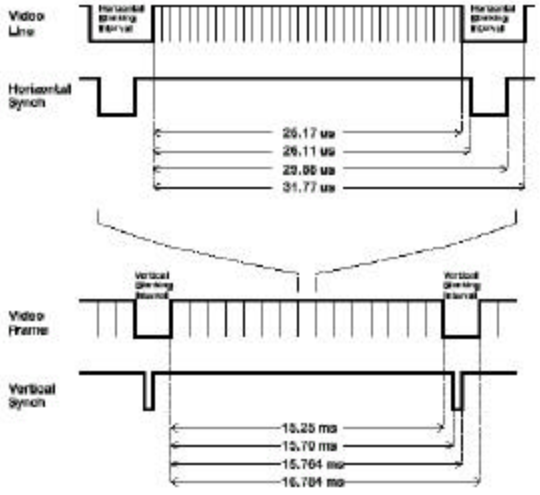


Figure 2: VGA signal timing.

Lab 5 Skeleton

- VGA Document at http://xess.com/appnotes/vga.pdf
  - Fair game for midterm #2
- Look at in Xilinx and demo it
  - VGA Sync module
  - Character ROM
  - Registered inputs (but really should register outputs)