Lecture #4: Programmable Logic Structure

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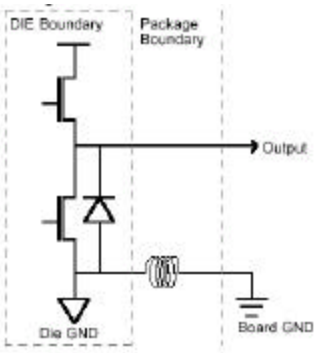
Book Reading

- Chapter 1
- Chapter 2.1-2.6
- Chapter 3.1.-3.7
- Chapter 4.1-4.3, 4.5
- Chapter 5.3, 5.4.1, 5.4.8, 5.5.1, 5.7.0, 5.8.1-5.8.4, 5.9.1-5.9.3, 5.10.1-5.10.7, 5.11.1
  - Know the architectures involved but don't need the TTL equivalents or ABEL/VHDL
- Chapter 10.5-10.6
  - Difference between CPLD and FPGA architecture

How do you drive a LED with CMOS?

- Point is that static power is used.
- Static power is a problem.
- Dynamic power has its issues as well.
- V=L*di/dt



Ground Bounce

- Mitigations
  - Internal Bypass Capacitors
  - More Power and Ground Pins
  - Lower Slew Rate of I/O
- More info:
  - http://www.idt.com/docs/AN_147.pdf

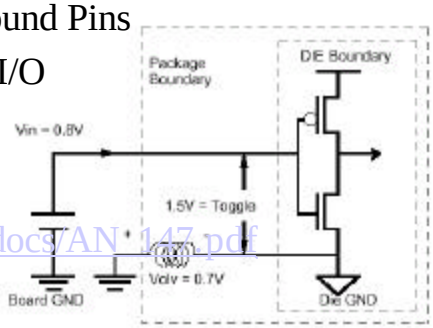
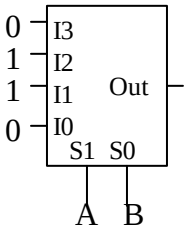


Figure 10, Volv = 0.7V can cause false switching

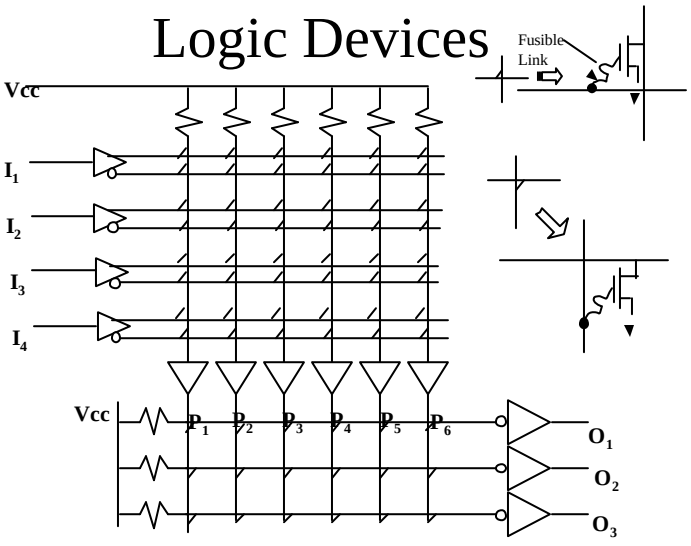
Mux as way to Implement Logic

- We did this in E40 and it's the same here
- Wired like this, small ROM
- If the inputs are configurable

Then basis for LookUp Table (LUT) FPGAs



Combinational Programmable Logic Devices

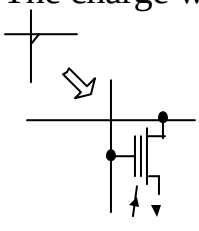


CPLDs (2)

- Burn in the interconnection to create logic
  - Uses wired logic but could be implemented with static CMOS
    - In Eetimes this week, Xilinx announced they are phasing out this architecture.
      - Too much power.

Erasable PLD

- Replace fuse with re-programmable device
  - Charge can be injected onto the floating gate thus turning the transistor off. The charge will remain on the gate even if the power is turned off. Later, if desired , the charge can be removed. The process is repeatable.



Floating gate

FPGAs

- Field Programmable Gate Arrays have a more general structure but based on these primitives.

FPGA Micro-Architecture

Xilinx Logic Cell Arrays General Chip Architecture:

- Lock Blocks (CLBs)
- IO Blocks (IOBs)
- Wiring Channels
- Other goodies (BlockRam)

- Use Data Books
- http://xilinx.com/partin

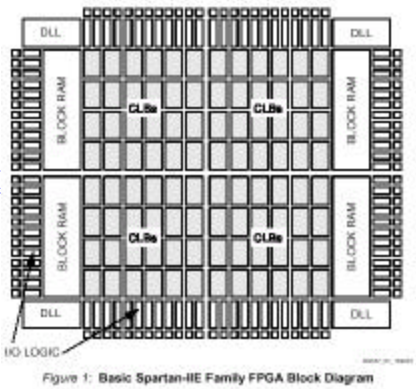
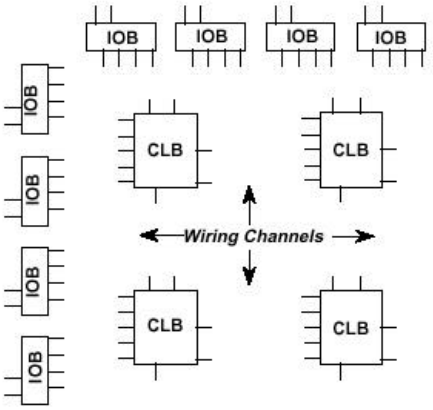


Figure 1: Basic Spartan-IIE Family FPGA Block Diagram

Wiring Channels

- Interconnect Logic created in FPGA to connect up logic
- Reconfigurable
- BIG FPGA feature



CLB Diagram From Data Book

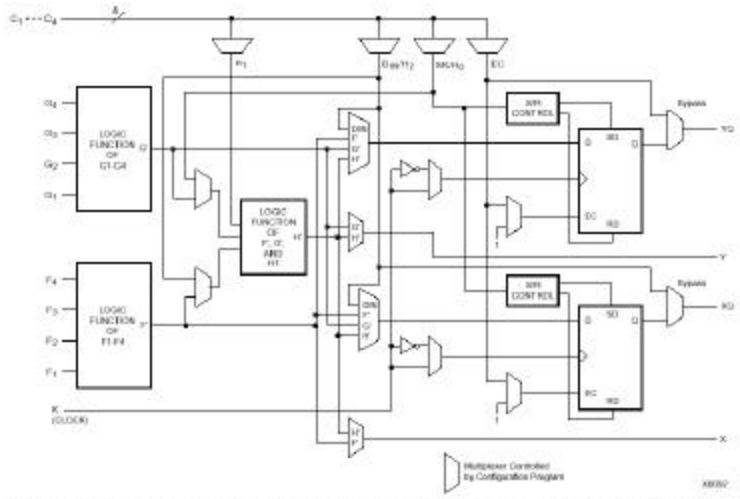


Figure 1: Simplified Block Diagram of XC4000 Series CLB (RAM and Carry Logic functions not shown)

IOB Diagram from Data Book

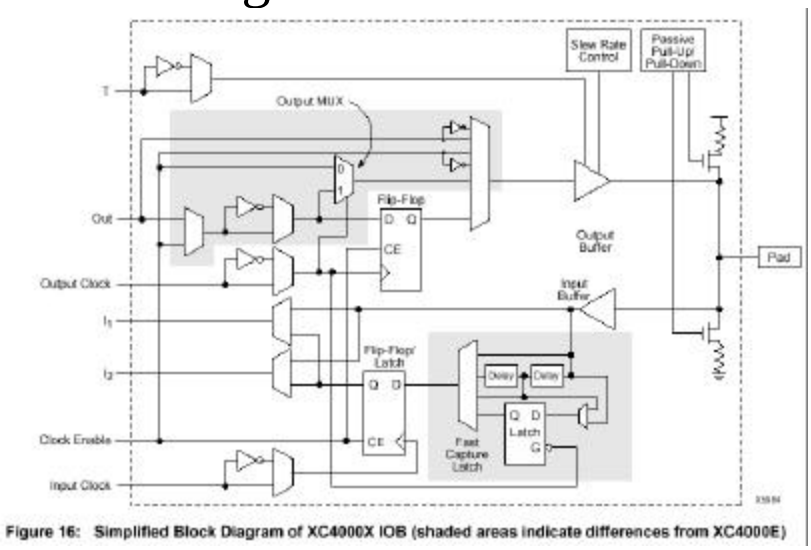


Figure 16: Simplified Block Diagram of XC4000X IOB (shaded areas indicate differences from XC4000E)

IOB Notes

- Note Tristate output driver
- Slew Rate control used to limit edge speed to lower instantaneous power (which affects ground bounce).
- Flip Flop at input so you don’t have to drive into interconnect.

Interconnect around CLBs

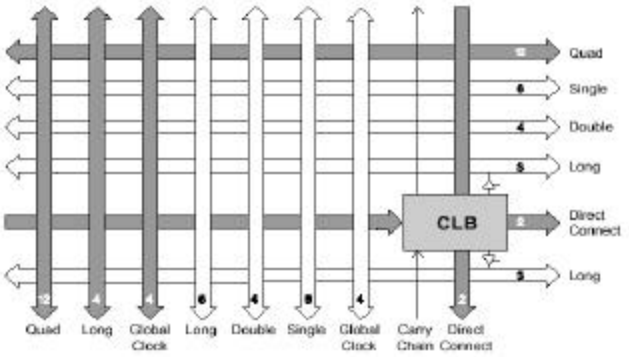


Figure 25: High-Level Routing Diagram of XC4000 Series CLB (shaded arrows indicate XC4000X only)

Programmable Switch Matrix

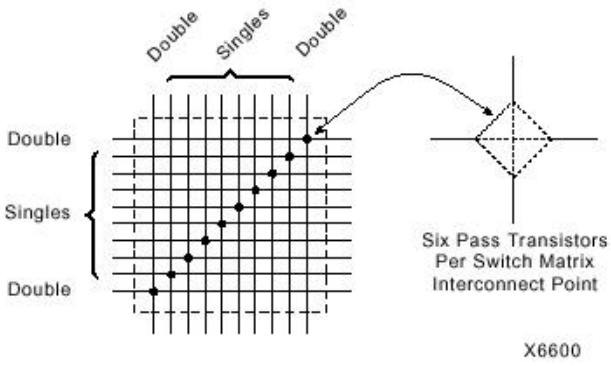


Figure 26: Programmable Switch Matrix (PSM)

More Routing

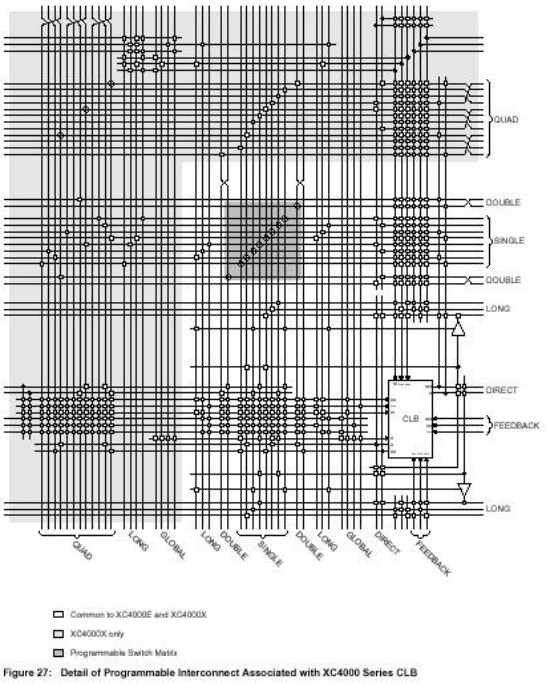


Figure 27: Detail of Programmable Interconnect Associated with XC4000 Series CLB

Last Routing Slide!! ☺

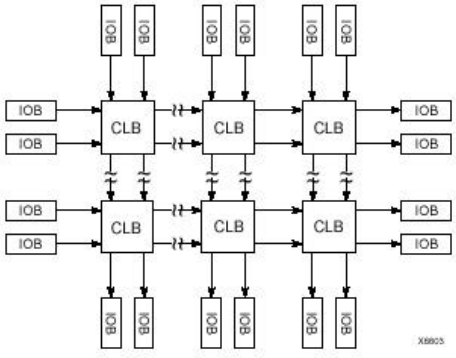


Figure 30: XC4000X Direct Interconnect

Timing Info

- http://xilinx.com/partinfo/ds005.pdf
- Use this info to guesstimate how fast design "should" run.

CLB Switching Characteristic Guidelines

Description	Symbol	Speed Grade -3 Min	-3 Max	-2 Min	-2 Max	-1 Min	-1 Max	-09 Min	-09 Max	-08 Min	-08 Max
Combinatorial Delays											
F/G inputs to X/Y outputs	T_{ILO}		1.6		1.5		1.3		1.2		1.1
F/G inputs via H' to X/Y outputs	T_{IHO}		2.7		2.4		2.2		2.0		1.9
F/G inputs via transparent latch to Q outputs	T_{ITO}		2.9		2.6		2.2		2.0		1.8
C inputs via SR/HO via H to X/Y outputs	T_{HHO}		2.5		2.2		2.0		1.8		1.8
C inputs via H1 via H to X/Y outputs	T_{HH1O}		2.4		2.1		1.9		1.6		1.5
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		2.5		2.2		2.0		1.8		1.8
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CRVP}		1.5		1.3		1.1		1.0		0.9

FPGA Figures of Merit

- FPGA operating frequency for your design is hard to predict beforehand.
- Run some micro-benchmarks on different FPGAs to get a feel for their perf and how much logic you can put between flip flops.
- 32 bit fast adder size and speed.

Understand FPGA Architecture

- Look up table (LUT) based with fixed and ***limited*** routing resources.
- So logic is cheap (consider 4 input XOR in VLSI) but wires are very expensive.
- FPGAs are manufactured in the same chip fabs as "high performance" ASICs based on standard CMOS. The tradeoff is easy of design vs performance.
  - Often a good tradeoff.