Lecture #3: Miscellaneous Logic Topics

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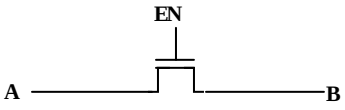
Administrivia

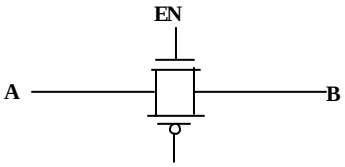
- Lab #1 & HW #1 due today
  - Any issues?
- Lab Section assignments online
  - No lab this week.
- Read Lab #2 before next week but light prelab.
- Review
  - Covered Boolean Algebra principles
  - Covered circuit design to support logic implementation

Transmission Gates

- This won't work…



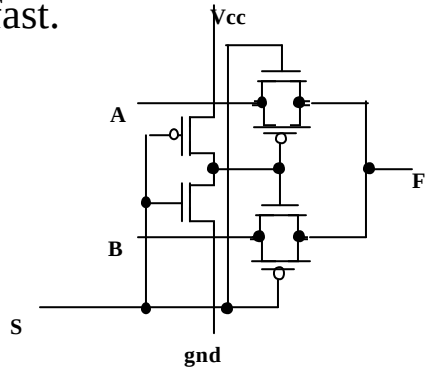
- Pass low's and high's equally well
  - Remember that it is Vg-Vs that determines whether or not a transistor is 'on'.



Transmission Gate As Mux

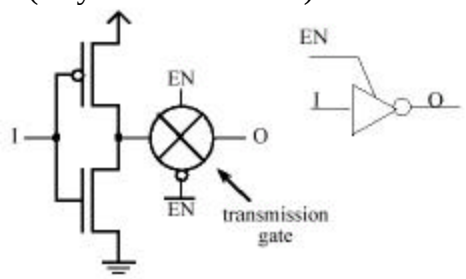
- Once Mux is set in one direction

propagation is very fast.



Tri-State Buffers

- Can you connect two drivers to one receiver?
  - Think of the PCI bus in you computer.
    - Share the data pins (they are 64 bits wide).

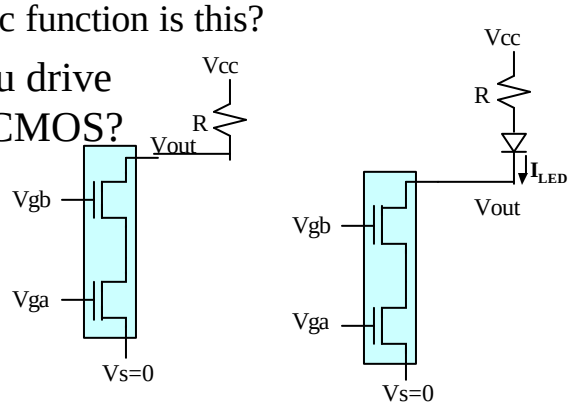


Tri-State Buffer

- How would we design it statically (ie, without the transmission gate).
  - Figure 3-48 in the book
- Power issues.
  - What if the turnon and turnoff times are the same?
- Most useful for chip I/O pins or design on board.
  - Generally don't use Tri-State logic inside chip.
    - Slow and powerful.
    - Use Mux tree since wiring not an issue
      - Area of active research.

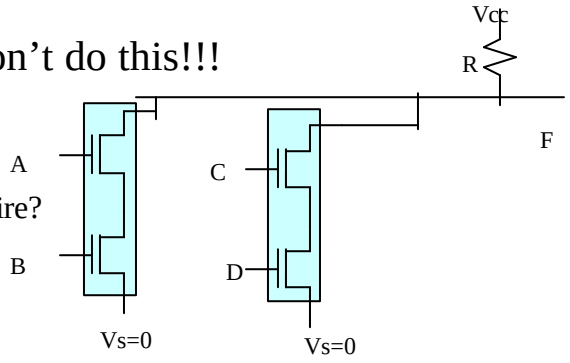
Open-Drain Outputs

- Not used too much anymore.
  - What logic function is this?
- How do you drive a led with CMOS?



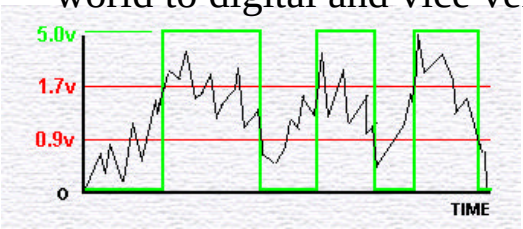
Wired Logic

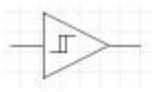
- What is F?
- In general don't do this!!!
  - Why?
    - Power
    - Wire as wire?



Schmitt-Trigger Inputs

- Hysteresis applied to logic circuits
  - Where else is hysteresis in EE?
  - Why does this work?
- Brings up whole issue of intefacing analog world to digital and vice versa



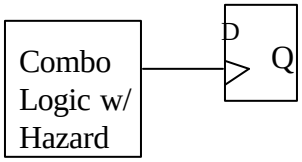


Logic Hazards

- Logic Hazards come from differences in propagation delay in a combinational circuit.
  - For SOP, make sure all the 1's in Kmap overlap
  - For POS, make sure all the 0's in Kmap overlap
    - Annoying but not difficult to compute…
- Not necessarily a bad thing.
  - Or more specifically when is it bad?

Gating the Clock?

- What if a potentially hazardous circuit drove a flip-flop
- This is ***BAD***!!
- Big lesson of this class:
  - Do Synchronous Logic Design unless you have a REALLY good reason to do something else.
  - So most combo circuits you design will be full of hazards but it won't matter.
- Need rules to make million gate desgns.
  - Compare to CS rules – goto is bad



Number Systems

- Binary[01], Decimal [0-9], Hex [0-9,A-F]
  - Know how to convert between them.
- IEEE standard defines the floating point format for numbers in computers (not in book).
  - More complicated than integer math
- One's Complement math is used for Cyclic Redundant Check (CRC) codes for network transmissions.

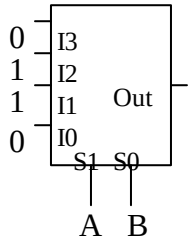
Two's Complement Arithmetic

- One's Complement (inverse) plus one
  - +12d = 1100b, -12d = 10100b
- Why do we have this weird system?
- Subtraction is the same as addition!
  - Assume you have an adder (we'll cover these later).
  - Adder is A + B
  - A + (-B + 1)
    - -B is simply a bank of inverters before the adder and +1 just sets the carry in to one of the LSB.
- Way Cool !!! ☺

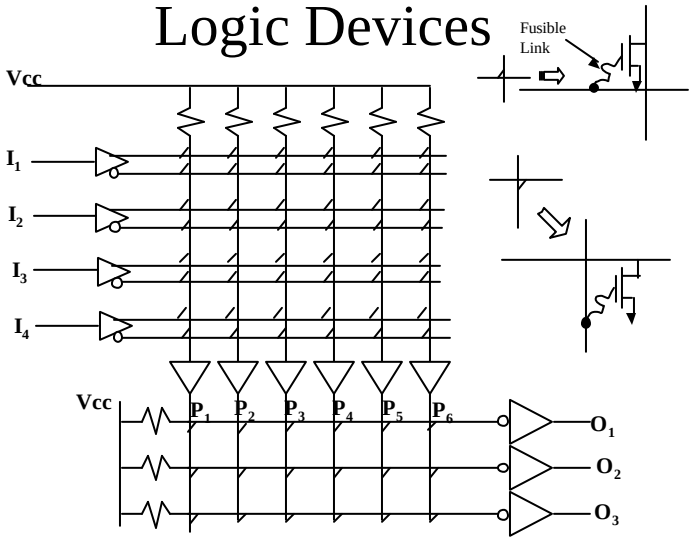
Mux as way to Implement Logic

- We did this in E40 and it's the same here
- Wired like this, small ROM
- If the inputs are configurable

Then basis for LookUp Table (LUT) FPGAs



Combinational Programmable Logic Devices

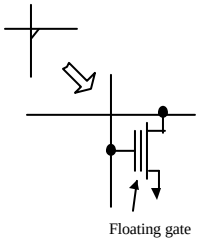


CPLDs (2)

- Burn in the interconnection to create logic
  - Uses wired logic but could be implemented with static CMOS
    - In Eetimes this week, Xilinx announced they are phasing out this architecture.
      - Too much power.

Erasable PLD

- Replace fuse with re-programmable device
  - Charge can be injected onto the floating gate thus turning the transistor off. The charge will remain on the gate even if the power is turned off. Later, if desired , the charge can be removed. The process is repeatable.



FPGAs

- Field Programmable Gate Arrays have a more general structure but based on these primitives