WELCOME TO EE121!

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Laboratory: Packard 127. Telephone: 725-1748.

Computer Cluster: Packard 128. Telephone: 725-1766.

Text: John F. Wakerly, *Digital Design Principles and Practice*s, third edition updated, Prentice Hall 2000. The third edition has several different printings, each of which corrects some typos and provides updated copies of the software. Any printing of the third edition is acceptable for this course. The second edition is outdated and we do not recommend using it.

Class resources:
We will use a class mailing list to send out important announcements about the class and the lab assignments. Make sure that you read these announcements carefully. We will add you the mailing list; do not try to subscribe yourself.

The class web page is http://eeclass.stanford.edu/ee121. You will be able to download handouts, read announcements, and view your grades on the web site.

Logic design and simulation software, Xilinx Foundation 2.1, is included with the text (after August 2000). But it is out-of-date and we recommend that you use version 4.1i instead. We will provide installation CDs on the first day of class from which you can install the software on your home computer. The software will also be available in the EE121 computer in Packard 128. You will have 24-hour access to the Packard building and the computer cluster, but not the lab.

Prerequisites: E40 or equivalent

Co-Requisite: E102E. All EE majors must take EE121 and E102E simultaneously. Anyone who wants to take E102E in a different quarter from E121 must petition the EE department.

Course content: Laboratories - 6 weekly labs during the first 7 weeks of the quarter
All labs except Lab 1 (to be done alone) are to be completed with one partner.

Lab descriptions will be distributed each week (no later than Tuesday).
Prelabs will be due *at the beginning of class* the following Tuesday.
Final Project - 3-week final project at the end of the quarter. You will design, construct, debug, and document a project with one partner. No late projects will be accepted. A writeup will be due approximately 2 days after your demonstration. This will be a challenging time. The final project demonstrations will be during the last week of classes.
Exams - two midterms
Grading

Assignment	Points
Lab 1	20
Lab 2	20
Lab 3	40
Lab 4	40
Lab 5	60
Lab 6	60
Homework (six or fewer)	10 each
Midterm 1	50
Midterm 2	50
Final Project	200
Final Project Write-up	50

Planned Course Outline

Labs:

Date(s)	Lab #	Topic	Readings
1/8-1/15	1	Xilinx Foundation Familiarization	Lab 1
1/15-1/22	2	Hardware Lab Familiarization	Lab 2
1/22-1/29	3	Combinational Circuits I	Lab 3
1/29-2/5	4	Combinational Circuits II	Lab 4
2/5-2/12	5	Sequential Circuits I	Lab 5
2/12-2/26	6	Sequential Circuits II	Lab 6
2/26-3/14	7	Final Project	Lab 7

Lectures:

1/8	Introduction	1.1-1.12, 3.1, 4.1
1/10	Combinational logic	4.2-4.3, 4.5, 5.1
1/15, 1/17	Implementation of Combin. Logic	3.4-3.8, 5.2, 10.5-10.6
1/22, 1/24	Special Combinational Circuits	5.4-5.4.5, 5.5-5.5.2, 5.6-5.8.4
1/29, 1/31	Intro to Sequential Circuits, State Machines	7.2-7.5
2/5	**Mid Term #1**	
2/7	Timing and Metastability	7.9, 8.8-8.9
2/12, 2/14	More Sequential Circuits	8.4, 8.5

2/19	State Machine Design	7.8, 8.7
2/21	Memories	10.1-10.4
2/26	Interfacing to Cores/SoC	
2/28	**Mid Term #2**	
3/5	HDLs/Verilog	
3/7	AD/DA Converters	
3/12	Bonus Topic	

Administrative Issues

EE121 is intended for undergraduate students who have taken E40. It is required for the EE and CSE majors, but could also be useful to students in other technical disciplines. It might also be appropriate for graduate students in technical disciplines other than EE. EE graduate students looking to improve their digital design skills should consider taking more advanced courses, such as EE183 (Advanced Logic Design Laboratory), EE271 (Introduction to VLSI Design), EE273 (Digital Systems Engineering), and EE275 (Logic Design). All students should be aware that EE121 is rewarding but time-consuming (especially during the final project), so be sure you have time in your schedule this quarter. Please talk to the TAs if you're not sure whether the course is right for you.

You must return to the TAs a completed class sign-up sheet. If you don't, you will be left off the class mailing list, will not have access to important features of the class web page, will not have access to Packard or the EE121 computer cluster, and will not be scheduled for a lab session. Please return it today after class even if you are not certain of your schedule. You can always submit a revised form later.

After we receive your sign up sheet, you will receive

1. 24-hour access to the Packard building and the EE121 computer cluster in Packard 128. You will use your SUID card to gain access to Packard and the computer cluster.
2. A login name and password that you can use to access the computers in Packard. A TA will e-mail these to you.
3. An assigned laboratory session. We will announce laboratory sessions next week.

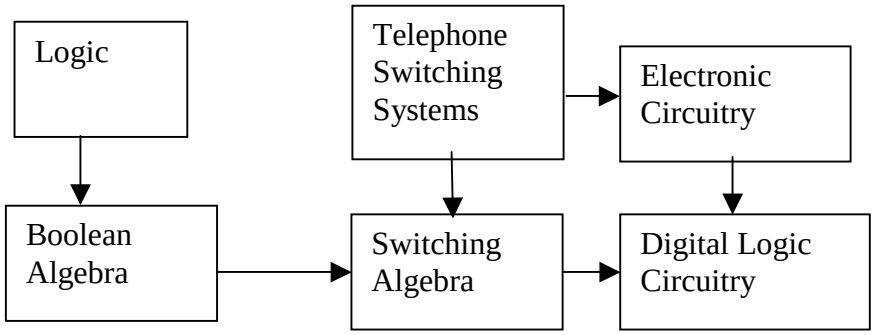
The EE department is using a new web-based tool called EEclass for its courses. Before you use the web site, you will need to register. Simply click on the "students" tab, then the "click here to register" link.

TA office hours for the first week ONLY will be

Sunday	7:30-9:30 PM	James
Monday	3:00-5:00 PM	Joel
Monday	7:00-9:00 PM	Lee

We will announce the permanent schedule next week. All office hours will be in Packard 127.

Introduction



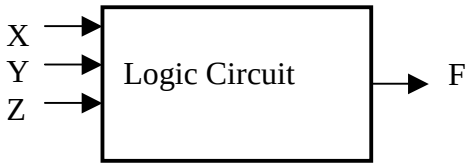
Binary digital logic covers up the shortcomings of the real, analog, world by representing the infinite set of values for a real quantity as a finite set of binary numbers or logic values.

Binary digit (bit): a logic value of 0 or 1. A set of n bits can represent 2^n possible values.

Logic values can be represented by a wide variety of physical phenomena: e.g. voltage (almost universal in this course), direction of magnetic domain, light, switch position, polarization direction, spin orientation, mechanical twist.

'Positive' logic: 'High' =1, 'Low' = 0. And vice versa for 'Negative' (not often used).

Buffer amplifier can be used to regenerate original logic (voltage) values for long distance communication.



Combinational circuit: F depends only on current values of X, Y, Z.

Sequential circuit: F depends on past values of inputs X,Y,Z , and may also depend on current values.

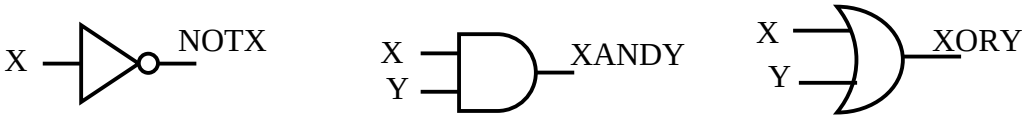
We will first concentrate on combinational circuits.

The operation of a combinational circuit can be described in a number of ways: e.g. the truth table:

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Any combinational circuit can be built from 3 basic "gates":

NOT AND OR

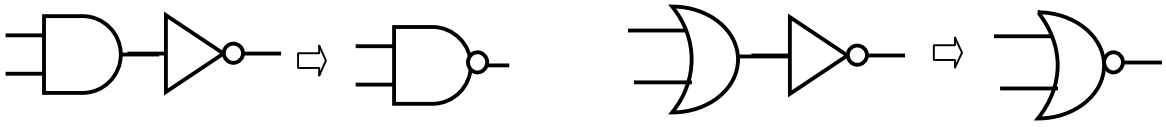


X	NOTX
0	1
1	0

X	Y	XANDY
0	0	0
0	1	0
1	0	0
1	1	1

X	Y	XORY
0	0	0
0	1	1
1	0	1
1	1	1

A NAND gates is simply AND followed by NOT ; and similarly for a NOR gate.



In most logic circuitry (at least for this course) NAND and NOR functions are more easily realized than are OR and AND.

Another feature of real logic circuitry is that it takes a non-zero time for the outputs to form.

Exercise:
How might you use the above gates to realize the functions?

X OR Y OR Z

X AND Y AND Z

X AND Y OR Z

Switching Algebra (Ch.4):
Defined by 5 pairs of axioms:

The first two pairs of axioms are:

1.	X= 0 if X≠1	X= 1 if X≠0
2.	If X= 0 then X' = 1.	If X= 1 then X' = 0.

We can write the AND operation X·Y and the OR operation X+Y thanks to their similarity with multiplication and addition (see the truth tables). This leads to the enormous convenience that we can set up rules that are similar to conventional algebra; in this case multiplication precedes addition so X AND Y OR Z becomes X·Y+Z = (X.Y)+Z; the ambiguity is resolved in the manner to which we are accustomed.

The remaining pairs of axioms are:

3.	0·0 = 0	1+1 = 1
4.	1·1 = 1	0+0 = 0
5.	0·1 = 1.0 = 0	1+0 = 0+1=1

The above 5 axioms lead to 11 pairs of theorems:

Single Variable Theorems:

1. Identities:	X+0 = X	X·1 = X
2. Null Elements:	X+1= 1	X.0 = 0
3. Idempotency:	X+X = X	X·X=X
4. Involution:	(X')' = X	(X') = X'
5. Complements:	X+X' = 1	X·X'= 0

These can be proved using ‘perfect induction’ starting from the axioms.

For example: To prove: X+ 0 = X
If X=1 then from axiom 5(R) X+ 0 = 1
If X=0 then from axiom 4(R) X+ 0 = 0
From axiom 1 these are the only two possible cases and in each case X+0=X. QED.

Two and 3-Variable Theorems
Can also be proved by perfect induction.

6.Commutative	$X+ Y = Y+ X$	$X\cdot Y = Y\cdot X$
7. Associative	$(X+Y) + Z = X+ (Y+Z)$	$(X\cdot Y)\cdot Z = X\cdot(Y\cdot Z)$
8. Distributive	$X\cdot Y+X\cdot Z = X\cdot(Y+Z)$	$(X+Y)\cdot(X+Z) = X+Y\cdot Z$
9. Covering	$X+X\cdot Y=X$	$X\cdot(X+Y) = X$
10. Combining	$X\cdot Y + X\cdot Y' = X$	$(X+Y)\cdot(X+Y') = X$
11. Consensus	$X\cdot Y+X'\cdot Z+Y\cdot Z = X\cdot Y+X'\cdot Z$	$(X+Y)\cdot(X'+Z)\cdot(Y+Z) = (X+Y)\cdot(X'+Z)$

We can replace variables (e.g. Y and Z) with expressions:

In T7 $(X+Y')+Z' = X+ (Y'+ Z')$

In T10 $(V'+X)\cdot(W.\ (Y'+Z)) + (V'+X)\cdot(W\cdot(Y'+Z))' = V'+X$

n-Variable Theorems
Can be proved by finite induction. That is, first prove for n=2; then prove that if the theorem is true for n= i it is also true for n= i+1.

12. Generalized Idempotency:
$X+X+\ldots..X = X$ $X\cdot X\ldots\ldots X = X$

13. DeMorgan $(X_1\cdot X_2\ldots..X_n)' = X_1' + X_2' +\ldots X_n'$ $(X_1+X_2+\ldots+X_n)'=X_1'\cdot X_2'\ldots X_n'$

14. Generalized DeMorgan
$[F(X_1,X_2\ldots..X_n, +,\cdot)]' = F(X_1', X_2' \ldots X_n', \cdot,+)$

15. Shannon's Expansion Theorem:
$F(X_1,X_2\ldots..X_n) = X_1\cdot F(1,X_2\ldots..X_n) + X_1'\cdot F(0,X_2\ldots..X_n)$

$=[X_1+F(0,X_2\ldots..X_n)]\cdot[X1'+F(1,X_2\ldots..X_n)]$

Duality

Any theorem or identity (in switching algebra) remains true when "0" and "1" are swapped and "·" and "+" are swapped throughout (*check the logic of this sentence*). This follows from the duality of the axiom pairs.

Put in appropriate brackets when exploiting duality otherwise you wind up with absurdities:

X + X·Y=X from T9
∴X'·X'+Y' = X' by duality
∴X'+Y' = X'

Representations of Logic Functions

Generalized Truth table for 3 variables:

Row	X	Y	Z	F	Minterm	Maxterm
0	0	0	0	F(0,0,0)	X'·Y'·Z'	X+Y+Z
1	0	0	1	F(0,0,1)	X'·Y'·Z	X+Y+Z'
2	0	1	0	F(0,1,0)	X'·Y·Z'	X+Y'+Z
3	1	1	1	F(0,1,1)	X'·Y·Z	X+Y'+Z'
4	1	0	0	F(1,0,0)	X·Y'·Z'	X'+Y+Z
5	1	0	1	F(1,0,1)	X·Y'·Z	X'+Y+Z'
6	1	1	0	F(1,1,0)	X·Y·Z'	X'+Y'+Z
7	1	1	1	F(1,1,1)	X·Y·Z	X'+Y'+Z'

minterm 7 maxterm 7

'Canonical sum' of a logic function: sum of minterms for which F=1.
'Canonical product': product of maxterms for which F=0

e.g. if F=1 for rows 0,3,4,6,7, then $F=\Sigma_{X,Y,Z}(0,3,4,6,7) = \Pi_{X,Y,Z}(1,2,5)$

'minterm list' or 'on-set' 'maxterm list' or 'off-set'