Stanford University
Department of Electrical Engineering

EE 121
Winter 2001-2002

Lab 5
VGA Ping Pong

Prelab Due Date: Tuesday, February 12, 2002 at 9:30am

1 Overview

This lab is to design and build a sequential circuit using a state machine, a shift register, and counters. This circuit will function as a simple ping-pong game. For the setup of the game, eight lights will represent a moving ping-pong ball and two pushbuttons will be used as "paddles." A single "on" light moves from left to right and "bounces" back from right to left if the right-hand player pushes the right pushbutton (RPB) when the ball is in the rightmost position---not too soon and not too late. Likewise, the left-hand player uses the left pushbutton (LPB) to hit the ball when it's in the leftmost position.

For this lab, there will be two ways to view the system outputs. A macro will be provided that will take the current ball position and the two scores and display them on the VGA monitor. In addition we will use the Xess board elements—bar led and seven segment displays—as alternate outputs. The two outputs should be in sync and comparing one to the other will help you debug your design during lab time.

The ping-pong circuit has the following input and output pins:

- **CLOCK** The onboard 25 MHz Xess Board Oscillator.
- **RESET** Master synchronous reset input.
- **LPB** Left paddle pushbutton input.
- **RPB** Right paddle pushbutton input.
- **L7-L0** Eight LED outputs that represent the ping-pong ball.
  L7 is the leftmost LED, and L0 is the rightmost.
- **SL6-SL0** Outputs to drive the left player's 7-segment score display.
- **SR6-SR0** Outputs to drive the right player's 7-segment score display.

Rules

The basic circuit plays ping-pong using rules that aren't exactly regulation play, but results in a fairly simple circuit design:

1) The rules are symmetric for the two players, L (left) and R (right).
2) The circuit knows who gets the next turn, L or R.
3) When it's L's turn, L hits the left paddle, LPB, and this starts the ball moving from left to right. Once the ball is moving from left to right, LPB is ignored.
4) When the ball is moving from left to right, R must push the right paddle, RPB, when

the ball is in the rightmost position. If R pushes RPB at this time, the direction of the ball changes, and it now moves from right to left. Now it's up to L to press LPB at the proper time.
5) If R pushes RPB before the ball is in the rightmost position, or fails to push RPB before the ball "falls off the end," then the turn ends, the ball disappears, L scores a point, and it's L's turn next.

SCOREKEEPING

NOTE: The schematics (which you should make into macros) for using the left and right 7-segment displays on the XStend boards will be provided to you. They will be available for download from the class web page.

Two 4-bit counters will be used to keep score, each feeding a 7-segment display. A player's maximum score should be limited to 9. The first player to 9 has won the game and their score should flash indicating they won. The game should stop until a user presses the reset button for another game.

OPTIONAL RULES **(May need extra states; do the basic system first)**

For your own edification, you may enhance your circuit to play by conventional rules. To do this, you must modify the rules given previously as follows:

a) The idea of taking turns is replaced with "serving." At any time, one player is designated to serve. The player who is serving is the one who starts the ball going. At the beginning of the game, L serves.

b) Only the player who is serving can score a point. If the player who was not serving misses the ball, the player who served scores a point and continues to serve.

c) If the player who served misses the ball, the other player serves next.

Suggest and test a simple external circuit change (i.e., one or two wires) that allows the ping-pong game to be played by a single human player L, where the other player R always returns the ball perfectly. Describe this in your README.

Laboratory Requirements

NOTE: This lab will take SUBSTANTIALLY more time than the previous labs, *SO START EARLY!!*

For this laboratory assignment, partners should work together.

There is one core state machine that controls the game state. For this state machine, use the synchronous sequential state machine design process discussed in class. You can use either binary or one-hot encoding.

A top-level schematic will be provided on the course web page that includes signal names and pin assignments. Please make sure that all signals defined in this file are still in your design.

NOTE: For all your logic blocks, you can use any of the elements in the Foundation library (including CoreGen) but ***you must not gate the clock***!!! This means that all state machines must be fully synchronous.

What to turn in for this week's Prelab:

1. Complete Foundation Project with schematics of all logic blocks in your design (submitted electronically)
2. Test script demonstrating that your design works (submitted electronically)
3. A report file that specifies resources used in the FPGA for the design—ie, the number of CLBs/IOBs/etc used. Look under the "reports" tab in Xilinx foundation. Summarize and discuss the results in your README in one paragraph (submitted electronically)
4. Extract timing information for the design as demonstrated in lecture and submit the file. The "Analyze against Auto Generated Design constraints…" button in the Xilinx Timing Analyzer tool will provide the values needed. Summarize and discuss the results in your README in one paragraph (submitted electronically)
5. Look at your design in the Xilinx FPGA Editor—be impressed it did all that wiring and not you! ☺ (JPEG screen dump submitted electronically)
6. Readme file (submitted electronically). Be sure to include a description of the single-player game.

Lab Exercise

During lab time, you will get a chance to compile your design, download it onto your Xilinx chip, and test it with real signals.

Submission

Submit this lab using the same instructions as for all previous labs.

Remember, you must submit your project electronically, whether or not it works correctly, before 9:30 AM on the due date or you will receive no credit.