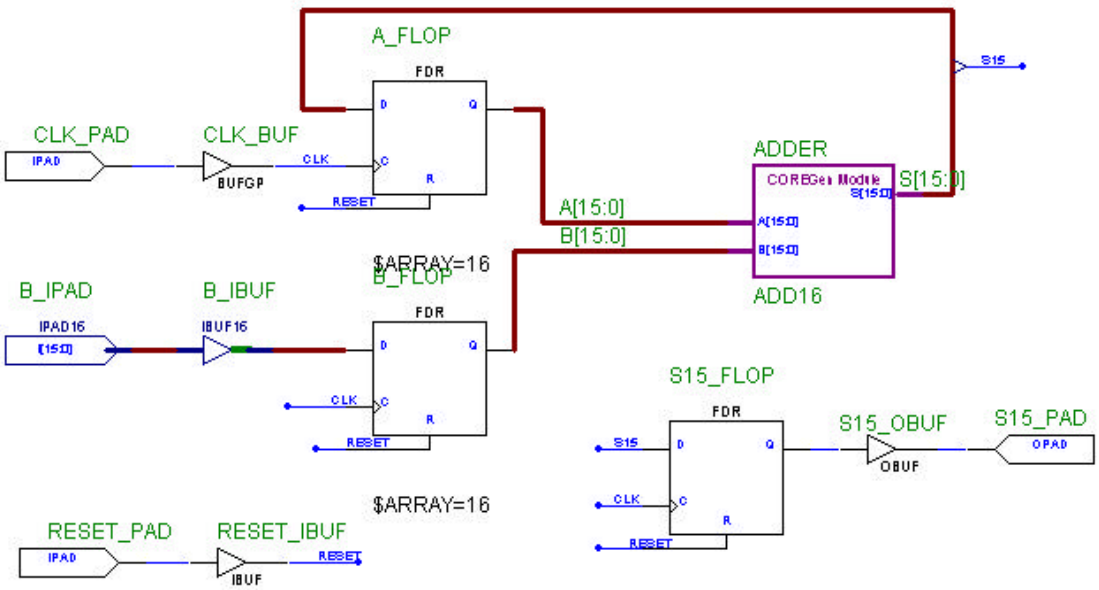
EE121: Homework #3
Winter 2001-2002
Assigned: Tuesday January 29, 2002
Due: Thursday February 7th, 2002 at 9:30am
NOTE: EE121 Midterm #1 is on Tuesday February 5th in class…
This assignment is worth 20 points or 2 HW equivalents.

For this assignment, you are going to extract some figures of merit for the Xilinx FPGA family and make some conclusions.

To do that, we want to measure the speed and size of various width adders in the XC2S100TQ144-5 Spartan II FPGA used on the boards in the EE121 lab.

Use the following schematic (available at the course website) as a template for the adder experiments.
The Xilinx Foundation tool will remove all unused/dead logic that is not on a path from input to output. In addition, we need to make sure that each design has a smaller number of IO pins than the number available (92 for our chip—a 32 bit adder would not meet this constraint: 2 32bit inputs + 1 32 bit output is 96 bits). These two constraints mean that we need to have all possible inputs connected to input pins. Question: Why is only S15 connected to an output pin?



To get actual data, measure the size and speed of the above design with a CoreGen adder of the following widths: 4, 8, 16, 32, 48, and 64. For each data point you will need a new schematic and CoreGen adder that has the same data width for all the components. The "total equivalent gate count" value in the "Map Report" is a good value to use for the size. To take the speed measurement, open the Xilinx Timing Analyzer and click on the stopwatch on the toolbar. The resulting timing report will have default measurement

values from auto-generated constraints. The "default period analysis for net CLK" is a good value for the design speed.

Plot both data sets (size and speed on y-axis and adder width in bits on x-axis) on a graph. Perform a linear regression on each data set to estimate the size and speed of a 24-bit adder. Is the relationship even linear? Either way, what might you conclude about the architecture CoreGen uses for the adder?

This FPGA comes in two speed grades: -5 "Standard Performance" and –6 "Higher Performance". [This is actually the name of –6!! ☺]. Approximate the speed advantage using the higher performance component.
You can accomplish this by rerunning the timing analyzer with the better speed grade. Plot the data on the same graph and run another linear regression. As you might expect, there is a difference in cost between the two speed grades. Check online for the cost differential between the two and compare the costs to the adder speed improvements. Hint: check the Xilinx website for Xilinx Distributors to get cost info. What is the expected performance of the 24-bit adder in the "higher performance" device?

The EE121 lab previously had boards with the Xilinx XS40-010XLPC84 FPGA
The marketing people told me our new chips are much faster, bigger (able to implement more logic) and cheaper. Measure and gather some data to support/refute these claims.

Provide several FPGA Editor snapshots in your report and comment on what they show. Specifically what do you see about the architecture that the CoreGen element occupies.

Create a HTML report and put it in your Leland space for this assignment. Send an email to your TA with the URL by the due date.

This assignment is to be done individually.

There are a lot of assumptions you have to make for this assignment. The goal is not to say that a certain FPGA is better or worse or to get exact/correct answers. It is to collect the above data and present it in a clear fashion so that a colleague can use the data. This type of process is often conducted to educate the other members of your team while in the investigative phases of a project.

I estimate that this assignment will take no more than 4 hours to do exactly what is requested. So put in a good faith, honor-code-backed, 4 hours and then turn in what you have but, at least, have something for each item requested.