EE 121 October 29, 2002
Digital Design Laboratory Handout #18

Midterm Examination #1

Open book, open notes. Time limit: 75 minutes

Honor Code Acceptance: This examination has been written according to the spirit and principles of the Stanford Honor Code.

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Signature

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Print Name

Problem	Score
#1	/ 20
#2	/ 25
#3	/ 30
#4	/ 30
Total	/ 105

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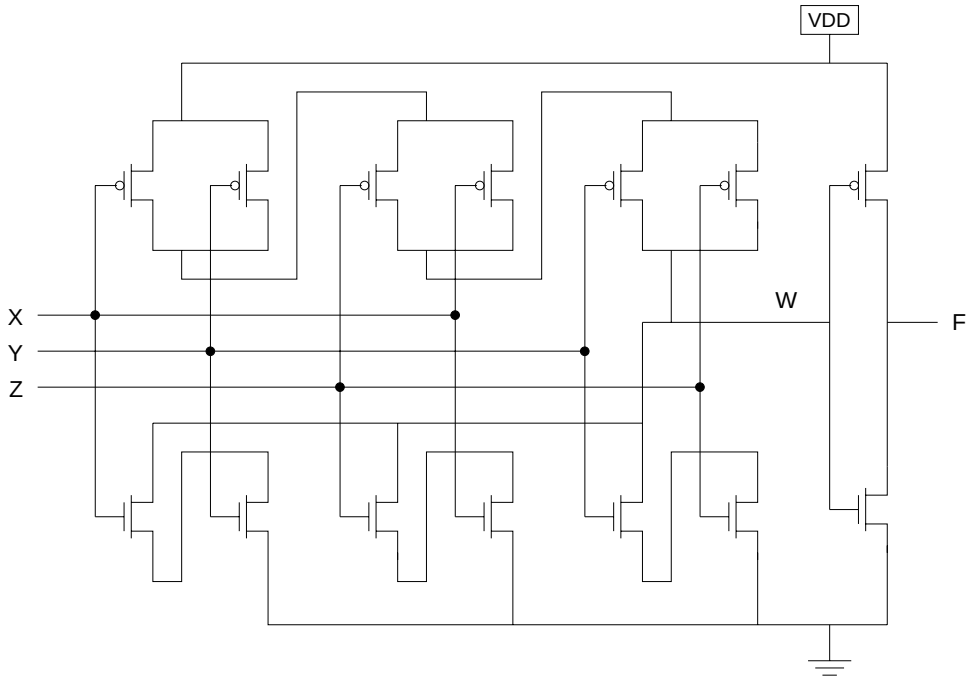
1. (20 points) *CMOS logic circuit.* The CMOS circuit show in the figure below computes a useful logic function.



a. Fill in the function table for the above circuit.

X	Y	Z	F
L	L	L	
L	L	H	
L	H	L	
L	H	H	
H	L	L	
H	L	H	
H	H	L	
H	H	H	

b. Describe briefly (*not* a Boolean formula) the function computed by the above circuit.

2. (25 points) *Combinational logic.* The exclusive-or of two variables is defined to be true when one input is true but not both. Exclusive-or can be generalized to three or more variables in several ways:

   XORnZ: true if exactly one input is true.

   XORnY: true if at least one input is true but not all inputs are true.

   XORn: true if an odd number of inputs is true.

   Only the last generalization is useful; for example, XOR3 is a component in a full adder.

   a. Find the minimal sum-of-products representation of XOR4Z.

   b. Find the minimal sum-of-products representation of XOR4Y.

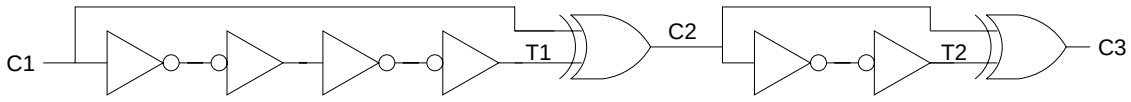
   c. Find the minimal product-of-sums representation of XOR4Y.

YZ \ WX	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

YZ \ WX	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

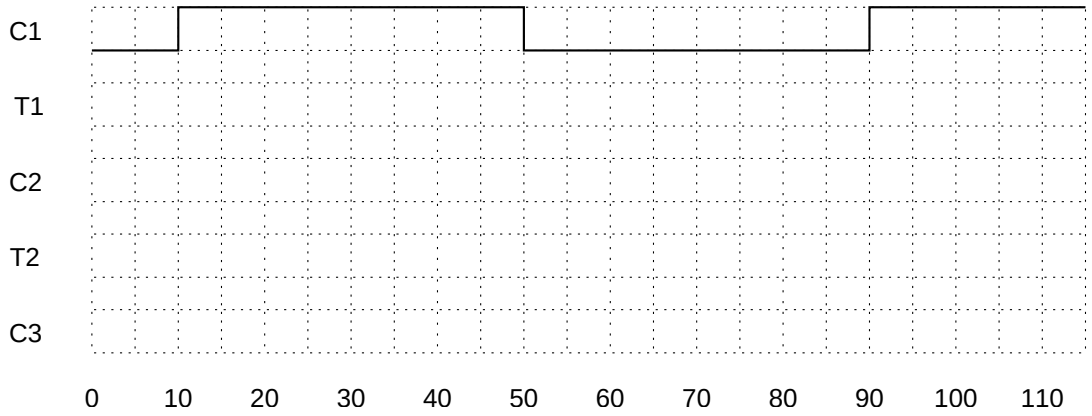
YZ \ WX	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

3. (30 points) *Glitches.* A devious circuit designer constructs the following circuit.



a. Find the Boolean formula for C3.

b. Suppose that the propagation delay for the inverters is exactly 5 ns and the propagation delay for the XORs is exactly 10 ns. Complete the following timing diagram.



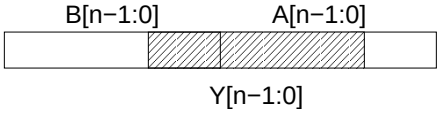
c. Using the result of part (b), describe the output C3 when the input C1 is a square wave with 80 ns clock period (12.5 MHz).

d. Suppose that the propagation delays are given by the following table:

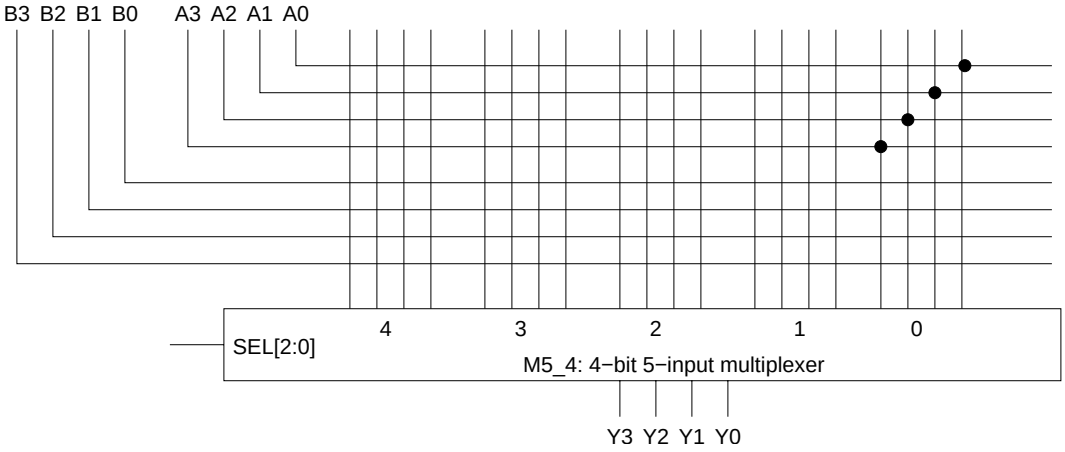
NOT		XOR	
$t_{\min} = 4$ ns	$t_{\max} = 6$ ns	$t_{\min} = 9$ ns	$t_{\max} = 12$ ns

Find minimum and maximum durations of the high pulses of intermediate signal C2.

4. (30 points) *Funnel shifter.* An n-bit *funnel shifter* is a combinational circuit that extracts n contiguous bits from the concatenation of two n-bit words, as shown below.



a. Complete the design of the following 4-bit funnel shifter by connecting input signals to multiplexer inputs. The *least* significant bit of the extracted field is specified by the multiplexer control inputs SEL[2:0], as shown by the signals connected to mux input 0.



b. A *logical left shift* SLL shifts an operand left, filling in the low-order bits with zeroes. For example, $\mathsf{SLL}(\mathsf{X[3:0]}, 2) = (\mathsf{X1}, \mathsf{X0}, 0, 0)$. To shift an input vector X[3:0] left, the input is connected to one of the funnel shifter inputs, A or B, and zeroes are supplied to the other input. Which input is X connected to?

c. What value of the control input SEL[2:0] is used to compute $\mathsf{SLL}(\mathsf{X}, 3)$?

d. A funnel shifter can also be used to *rotate* a 4-bit operand, by connecting the input operand to both data inputs of the funnel shifter. What control value SEL[2:0] is used to produce the left rotation $\mathsf{ROL}(\mathsf{X[3:0]}, 1) = (\mathsf{X2}, \mathsf{X1}, \mathsf{X0}, \mathsf{X3})$?