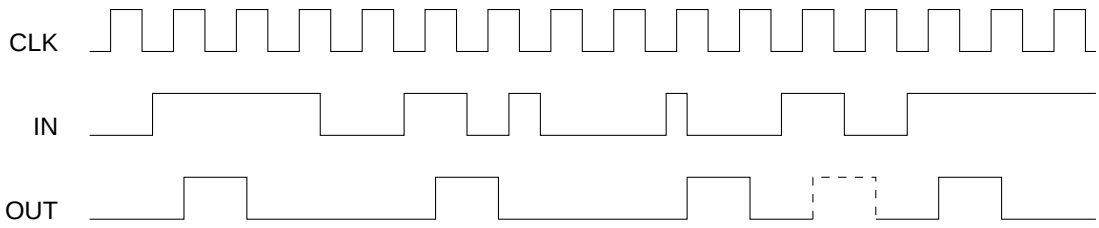
Topics for Lecture #9

- Reminder: midterm examination #1 next Tuesday starting at 9:30am.
- Examples of small state machines
  - simultaneous button push detector (continued)
  - button push processor
  - pulse stretcher
- General procedure for state machine design
- Counters: definitions, examples, applications

Button input processor

Requirement: output a pulse of duration one clock period in response to each input pulse.

Example of desired behavior.



The dashed pulse corresponds to an ambiguity in the specifications: how should this state machine respond to consecutive short input pulses?

In some applications consecutive pulses will not or should not occur, so this possibility can be ignored.

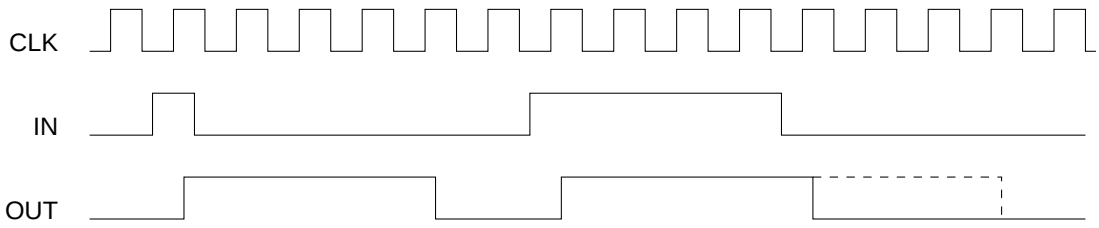
Button input processor (2)

State machines and transition/output tables.

Pulse stretcher

Requirement: each input pulse produces a 4-clock output pulse.

Example of desired behavior:

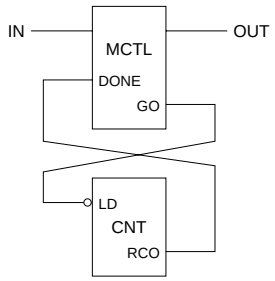


These specifications are also ambiguous: is the output *retriggerable*? Can output pulses be longer than 4 clocks?

Pulse stretcher (2)

State machines and transition/output tables.

The circuit can be simplified by decomposing into two state machines.



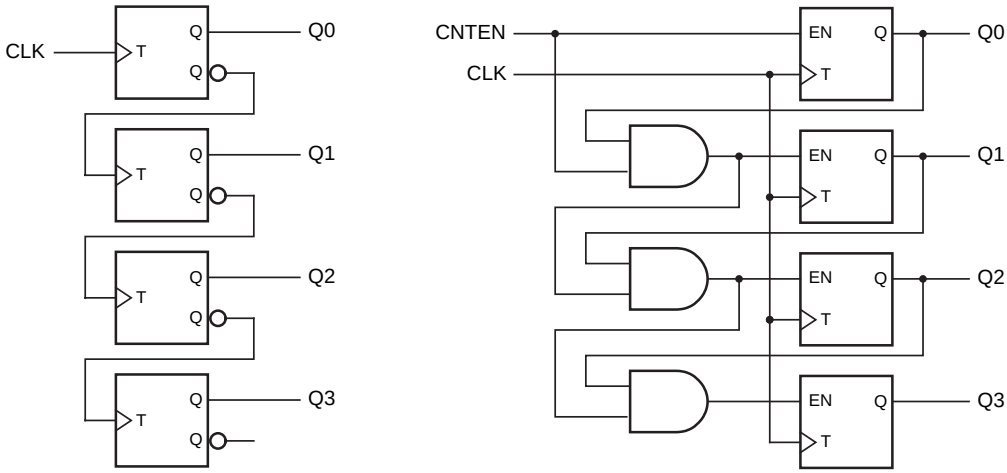
State machine design

0. Specify desired behavior of machine unambiguously (often hardest step).
1. Construct state/output table (or draw a state diagram, often preferable).
2. Minimize the number of states (optional).
3. State assignment: choose state variables and assign values to named states.
4. Form transition/output table from state/output table using state values.
5. Choose flip-flop type. Answer: D flip-flops
6. Construct excitation table (not needed for D flip-flops)
7. Derive excitation equations from excitation table.
8. Derive output equations from transition/output table.
9. Draw logic diagram of next-state logic (or provide equations to CAD tools).

Counter uses

- Real time clock: cycle through a sequence of states in a known order. State encodings: binary, BCD = binary coded decimal, Gray.
- Frequency divider: output a period signal at a fraction of input frequency.
- Event counter: increment state each time a signal or Boolean function is true (on rising edge of clock).
- Interval timer: count number of clock pulses between start and stop signals
- Alarm clock: activate an alarm signal at a specified time in the future.
- Delay: activate a timeout signal after a specified number of clock cycles.

Ripple vs. synchronous counter

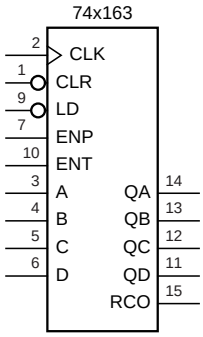


Ripple counter: each bit toggles when lower order bit changes from 1 to 0.

Synchronous: a bit changes at rising clock edge when all lower bits are 1.

74x163 binary synchronous counter

Logic symbol:



Next-state logic and output logic for the 74x163:

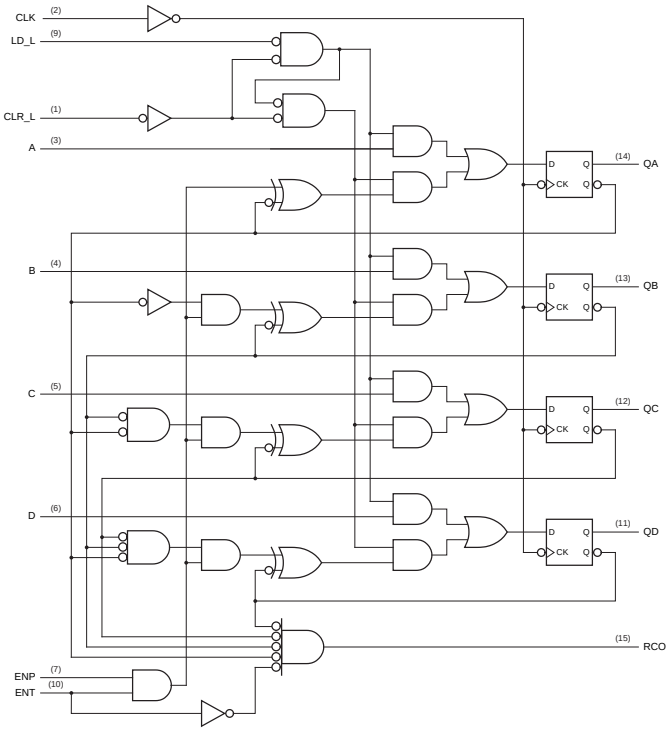
```
[QD,QC,CB,QA] :=
  if CLR then [0,0,0,0]
  else if LD then [D,C,B,A]
  else if ENP * ENT then [QD,QC,CB,QA] + [0,0,0,1]
  else [QD,QC,CB,QA];
RCO = ENT * QD * QC * QB * QA;
```


74x163 state table

Table 8-11 State table for a 74x163 4-bit binary counter.

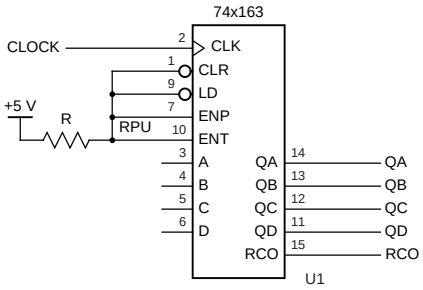
Inputs				*Current State*				*Next State*			
CLR_L	*LD_L*	*ENT*	*ENP*	*QD*	*QC*	*QB*	*QA*	*QD**	*QC**	*QB**	*QA**
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	QD	QC	QB	QA
1	1	x	0	x	x	x	x	QD	QC	QB	QA
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

74x163 logic diagram

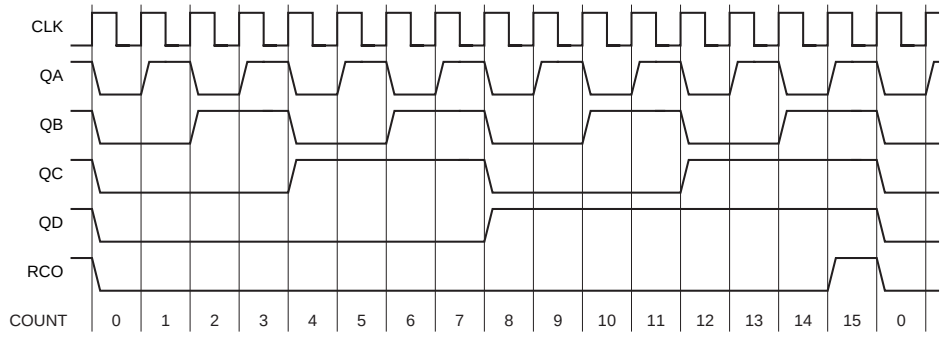


74x163: free-running counter

Connections:

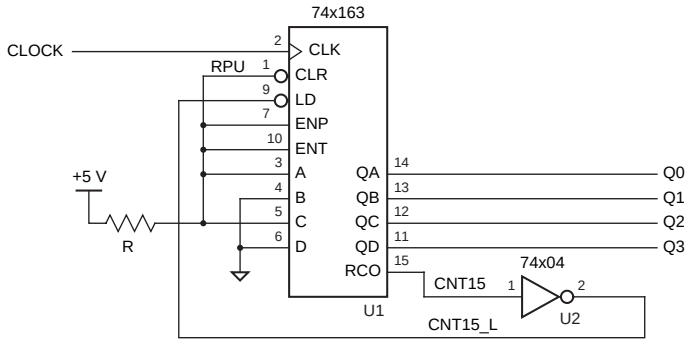


Timing diagram for divide-by-16 counter

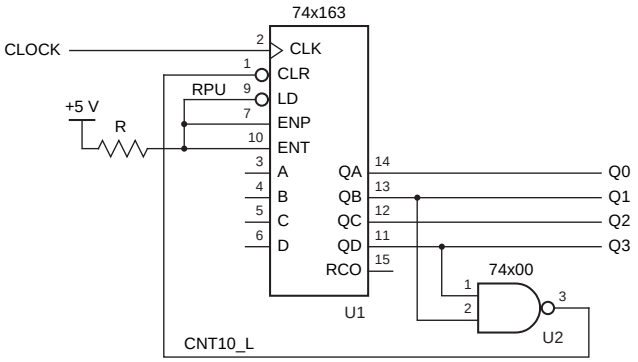


Modulo-11 counters

State sequence:
5, 6, . . . , 15, 5 . . .

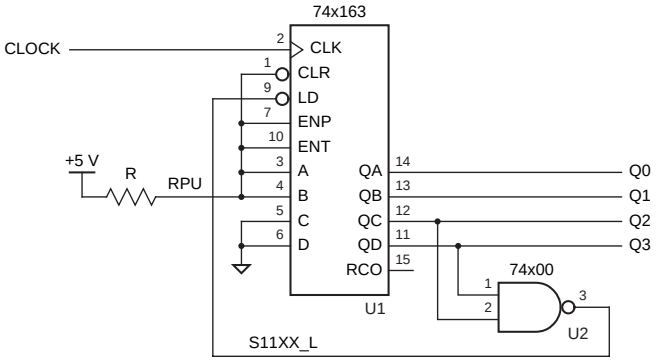


State sequence:
0, 1, . . . , 10, 1 . . .



Excess-3 decimal counter

State sequence:
3, 4, . . . , 11, 12, 3. . .

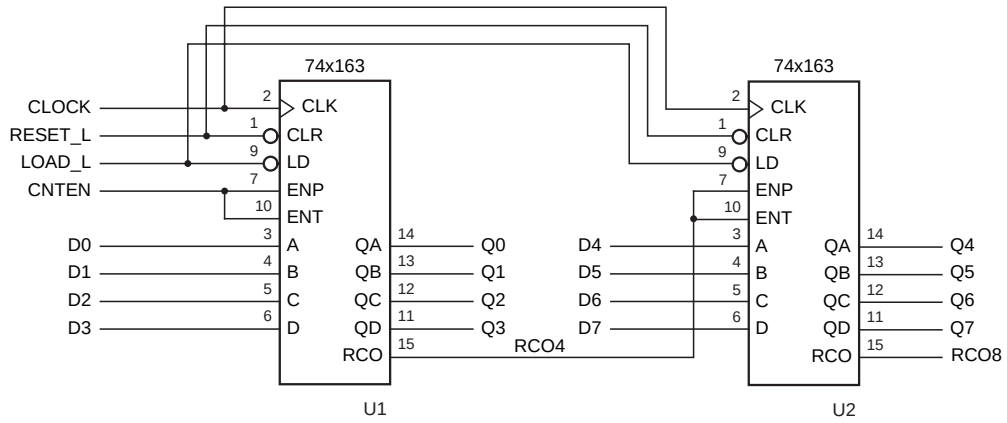


With one 3-input NAND gate, any period between 1 and 16 can be obtained.

In fact, any low and high values can be specified.

Drawback of 74x163: counts up only. Use 74x169 for bidirectional counting.

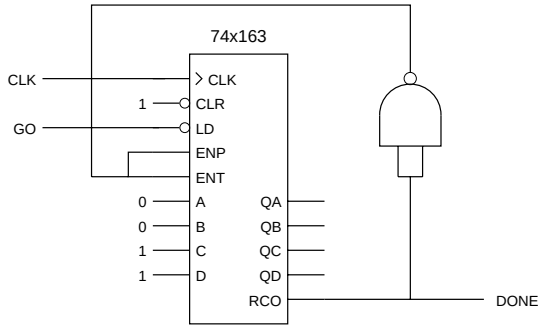
Cascaded binary counters



Important: do not use RCO as a clock. RCO may (will) glitch.

RCO should be used to enable the next counter, i.e., to tell the next counter when to increment on the next active clock edge.

Delay submachine using 74x163



DONE is asserted four clocks after GO is asserted.