Canonical Boolean function representation

Five canonical representations are described in the textbook:

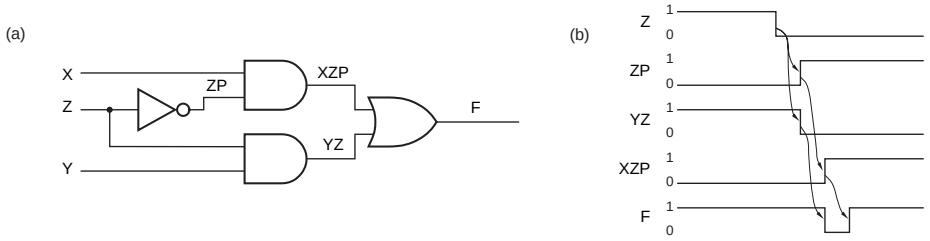
- truth table
- canonical sum
- minterm list
- canonical product
- maxterm list

Representations 4 and 5 are *duals* of 2 and 3.

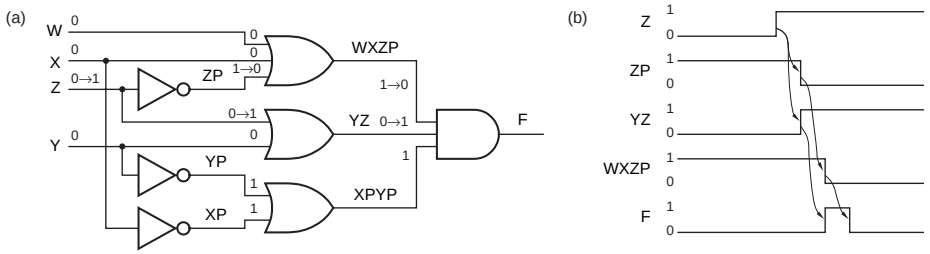
Most people find it difficult to think in terms of products of sums, but CAD programs manage quite nicely.

Timing hazards

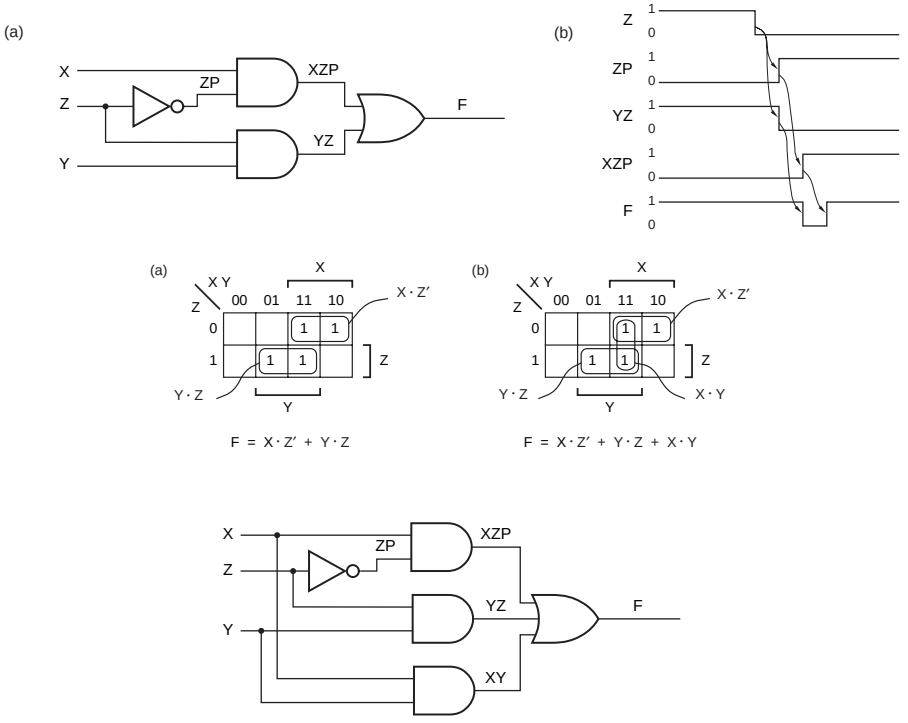
Sum of products: static-1 hazard:



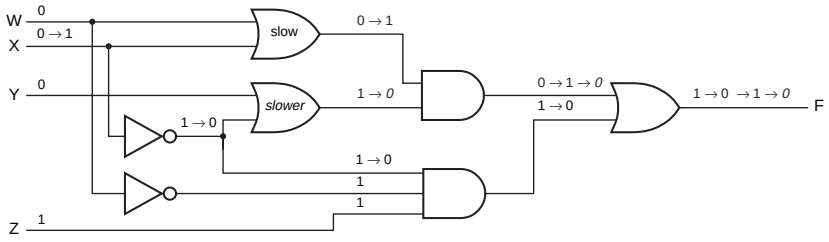
Product of sums: static-0 hazard:



Hazards and Karnaugh maps



Dynamic timing hazards



Signal names and active levels

Some inputs and outputs are "active" (cause something to happen) when their voltage level is low. These signals are called "active-low."

Most logic circuits contain a mixture of active-high and active-low signals.

One reason: simplest gates (NAND, NOR, NOT) are inverting.

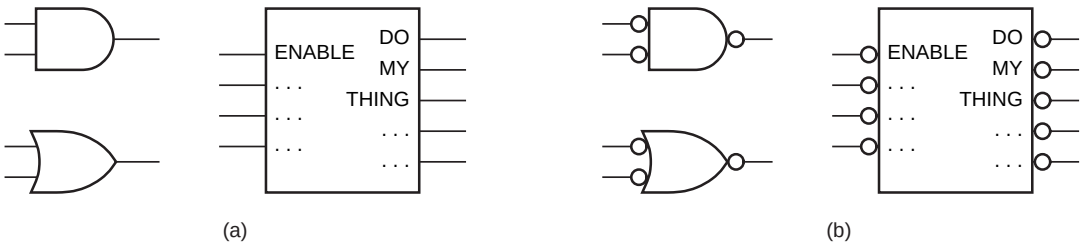
Signal names should when possible indicate the active level of the signal.

Table 5-1
Each line shows a different naming convention for active levels.

Active Low	*Active High*
READY–	READY+
ERROR.L	ERROR.H
ADDR15(L)	ADDR15(H)
RESET*	RESET
ENABLE~	ENABLE
~GO	GO
/RECEIVE	RECEIVE
TRANSMIT_L	TRANSMIT

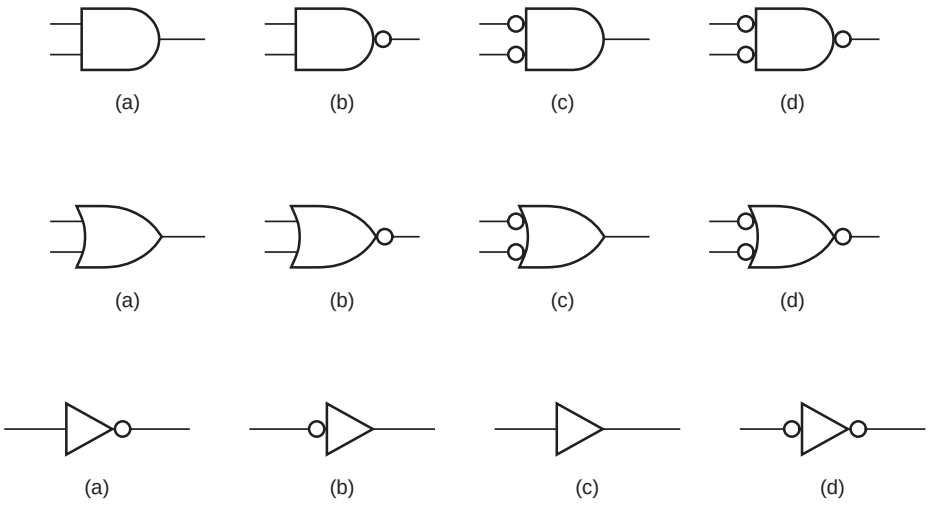
Bubbles

Active-low input and output signals are indicated by bubbles:



Bubbles (2)

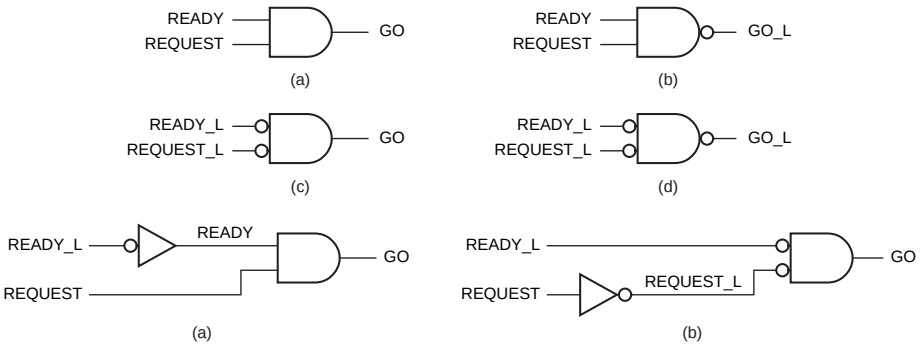
The same conceptual function (AND, OR, NOT) can be implemented by different gates, depending on active level of inputs and outputs.



Bubble-to-bubble logic design

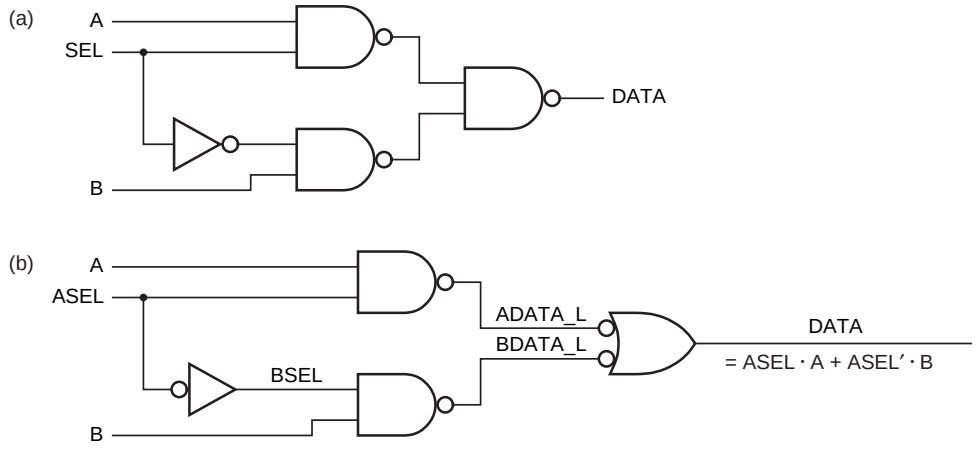
Ideally, active-low signals should connect to bubbles on gates.

(We cannot always match active-low signals to bubbles: e.g., $Y = A \cdot B'$.)



Bubble-to-bubble logic design (2)

Bad schematic and good schematic for NAND-NAND circuit:

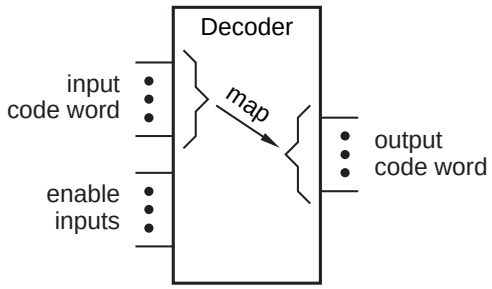


Combinational Logic Building Blocks

- decoder
- multiplexer
- encoder
- comparator
- adder

Decoder

Decoder converts input code to output code.



Input coding is usually more compressed than output coding.

E.g., output coding may be 1-out-of-m.

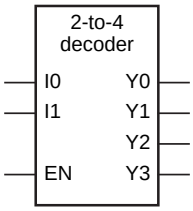
Most compact encoding is binary: m signals represent 2^m possible outcomes.

Unless enabled by ENABLE inputs, no outputs are true.

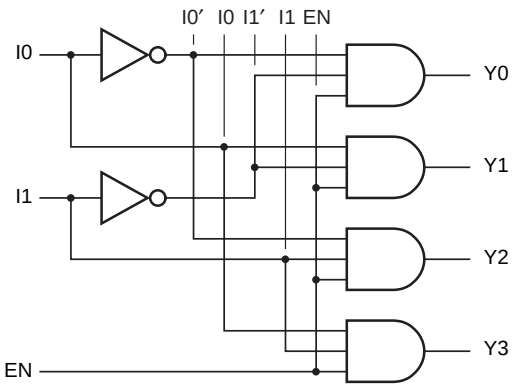
2-to-4 decoder with enable

Table 5-4
Truth table for a 2-to-4 binary decoder.

Inputs			*Outputs*			
EN	I1	I0	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0



(a)

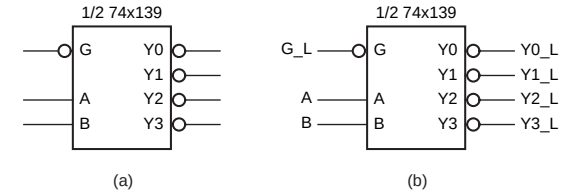


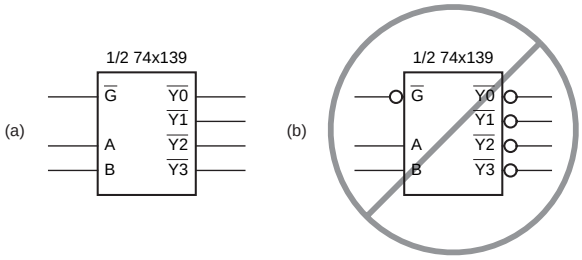
(b)

74x139 dual 2-to-4 decoder

Table 5-6 Truth table for one-half of a 74x139 dual 2-to-4 decoder.

Inputs			Outputs			
G_L	B	A	Y3_L	Y2_L	Y1_L	Y0_L
1	x	x	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1





74x138 3-to-8 decoder: symbol and schematic