Representations of bits

Table 3-1 Physical states representing bits in different computer logic and memory technologies.

Technology	State Representing Bit	
	0	1
Pneumatic logic	Fluid at low pressure	Fluid at high pressure
Relay logic	Circuit open	Circuit closed
Complementary metal-oxide semiconductor (CMOS) logic	0–1.5 V	3.5–5.0 V
Transistor-transistor logic (TTL)	0–0.8 V	2.0–5.0 V
Fiber optics	Light off	Light on
Dynamic memory	Capacitor discharged	Capacitor charged
Nonvolatile, erasable memory	Electrons trapped	Electrons released
Bipolar read-only memory	Fuse blown	Fuse intact
Bubble memory	No magnetic bubble	Bubble present
Magnetic tape or disk	Flux direction “north”	Flux direction “south”
Polymer memory	Molecule in state A	Molecule in state B
Read-only compact disc	No pit	Pit
Rewriteable compact disc	Dye in crystalline state	Dye in noncrystalline state

Not all logic *representations* are suitable for logic *gates*.

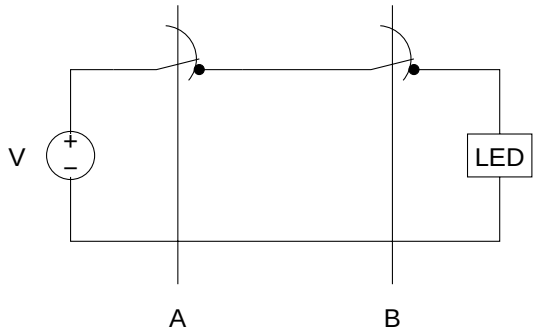
Logic device must outputs that are of the same type as its inputs.

AND and OR gates using switches

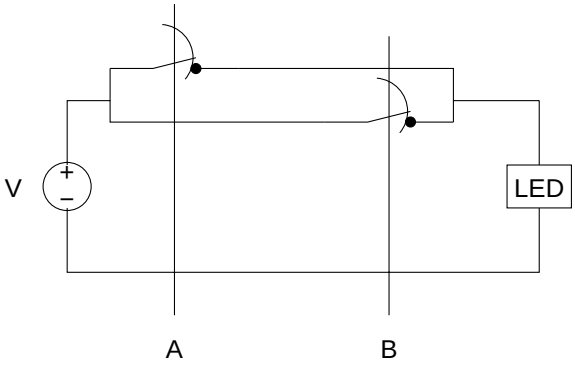
Single-pole single-throw (SPST) switches are either normally open (n.o.) or normally closed (n.c.).

Normally-open switches can be used to build AND and OR gates.

AND gate: serial connection:



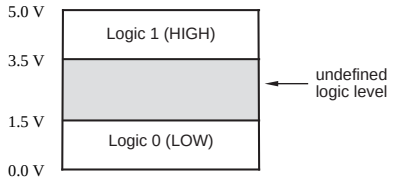
OR gate: parallel connection:



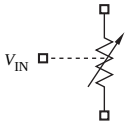
MOS transistors

Logic levels for CMOS circuits have wide range, from $> 12\,\text{V}$ down to $\sim 1\,\text{V}$.

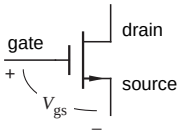
Often 5 V is used for compatibility with older logic families (TTL).



MOS transistors are voltage-controlled resistances that we use as switches.

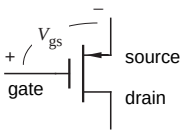


n-type transistors are normally open; p-type transistors are normally closed.



Voltage-controlled resistance:
increase V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \geq 0$

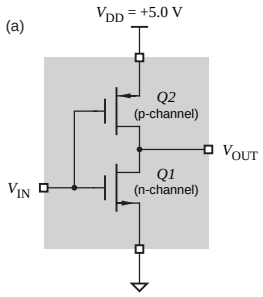


Voltage-controlled resistance:
decrease V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \leq 0$

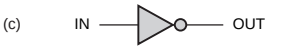
CMOS inverter

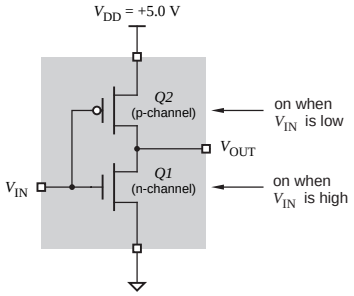
Schematic, function table, and logic symbol:



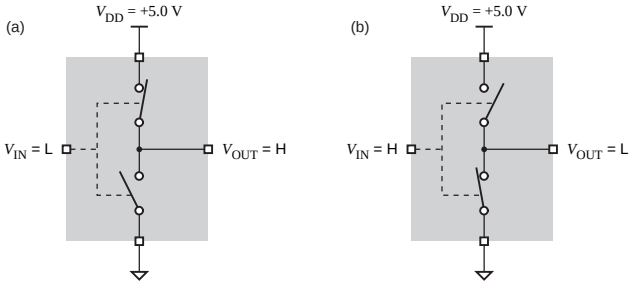
(b)

V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)



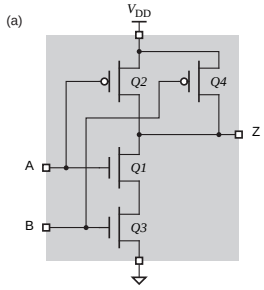


Switch view of CMOS inverter:



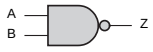
CMOS NAND

Schematic, function table, and logic symbol:

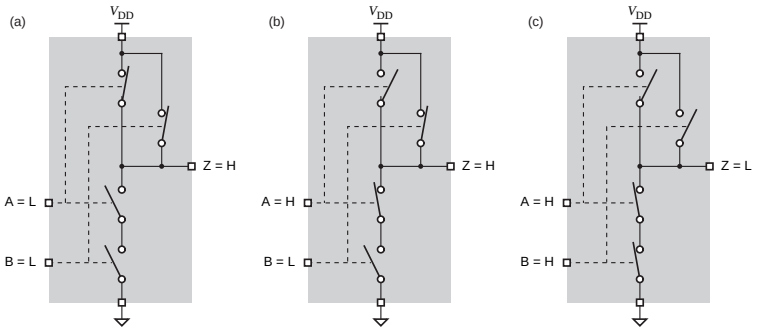


(b)

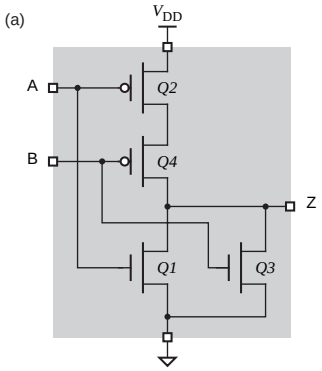
A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L



Switch models for CMOS NAND gate:

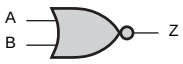


CMOS NOR



(b)

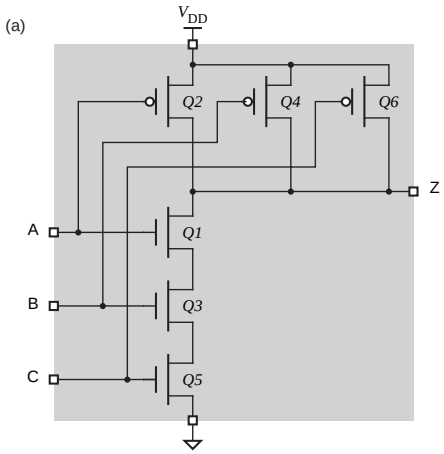
A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L



NAND and NOR are *dual* Boolean functions (to be discussed later). Their logic circuits are dual circuits.

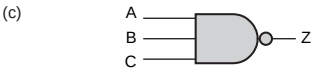
Performance of NAND or NOR is not the same because pMOS and nMOS transistors have different characteristics. CMOS NAND gates are faster than NOR gates because of series connnection of n-channel transistors has higher conductance than series connection of p-channel transistors.

n-input NAND and NOR



(b)

A	B	C	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	Z
L	L	L	off	on	off	on	off	on	H
L	L	H	off	on	off	on	on	off	H
L	H	L	off	on	on	off	off	on	H
L	H	H	off	on	on	off	on	off	H
H	L	L	on	off	off	on	off	on	H
H	L	H	on	off	off	on	on	off	H
H	H	L	on	off	on	off	off	on	H
H	H	H	on	off	on	off	on	off	L



This implementation of n-input NAND or NOR uses n pairs of transistors.

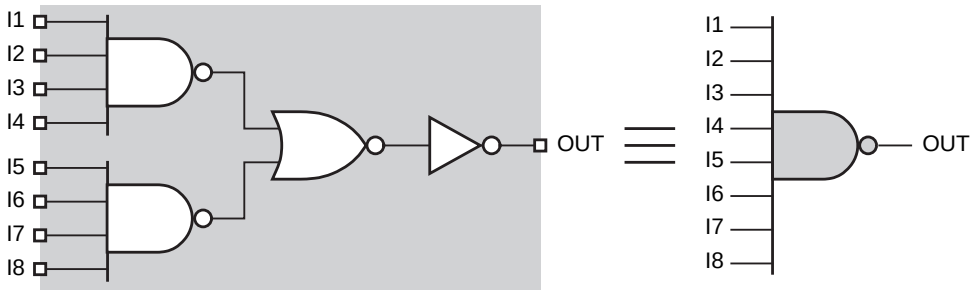
Unfortunately, delay increases with the number of inputs:

$$\text{delay} \approx a + bn^2$$

Large fan-in gates

For a large number of inputs, it is faster to use multiple gates.

Example: 8-input NAND might be faster using three small gate delays.

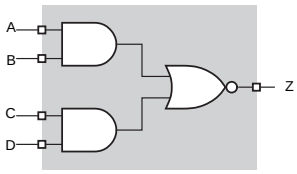


Note the tradeoff between speed and cost: 22 transistors vs. 16 transistors.

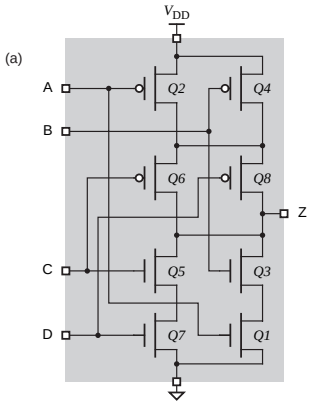
Cost is proportional to the number of transistors or area in integrated circuit.

CMOS AND-OR-INVERT

The circuit below uses two AND gates ($2 \cdot 6 = 12$T) and one NOR gate (4T).



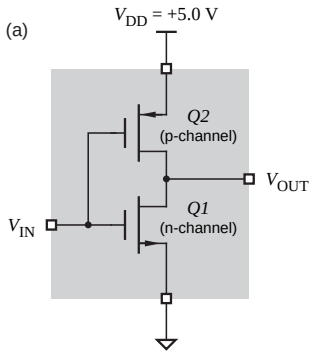
This logic function can be implemented directly using 8 transistors.



(b)

A	B	C	D	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	*Q7*	*Q8*	Z
L	L	L	L	off	on	off	on	off	on	off	on	H
L	L	L	H	off	on	off	on	off	on	on	off	H
L	L	H	L	off	on	off	on	on	off	off	on	H
L	L	H	H	off	on	off	on	on	off	on	off	L
L	H	L	L	off	on	on	off	off	on	off	on	H
L	H	L	H	off	on	on	off	off	on	on	off	H
L	H	H	L	off	on	on	off	on	off	off	on	H
L	H	H	H	off	on	on	off	on	off	on	off	L
H	L	L	L	on	off	off	on	off	on	off	on	H
H	L	L	H	on	off	off	on	off	on	on	off	H
H	L	H	L	on	off	off	on	on	off	off	on	H
H	L	H	H	on	off	off	on	on	off	on	off	L
H	H	L	L	on	off	on	off	off	on	off	on	L
H	H	L	H	on	off	on	off	off	on	on	off	L
H	H	H	L	on	off	on	off	on	off	off	on	L
H	H	H	H	on	off	on	off	on	off	on	off	L

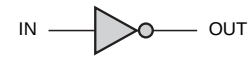
CMOS steady-state electrical behavior

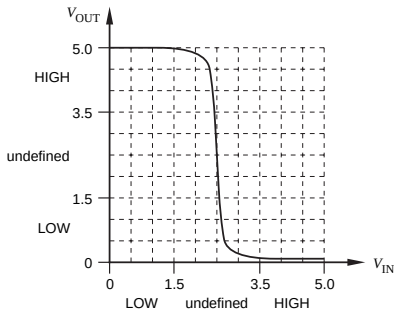


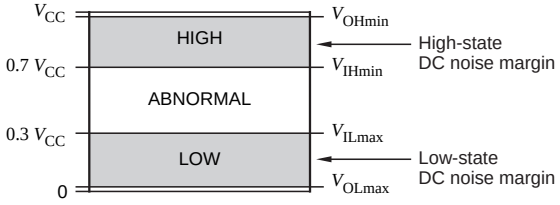
(b)

V_{IN}	*Q1*	*Q2*	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

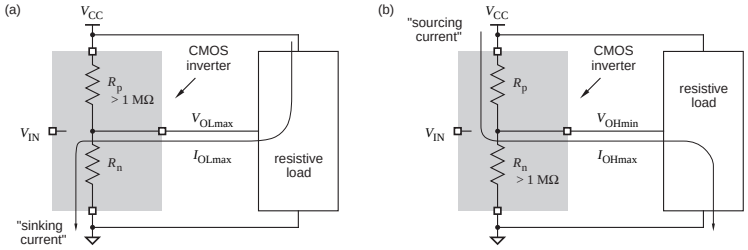
(c)







Resistive loads, nonideal inputs

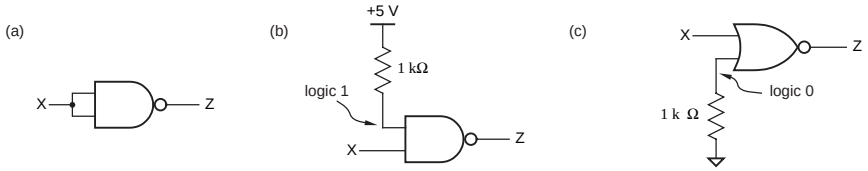


Output voltage will differ from ideal high or low if too much output current.

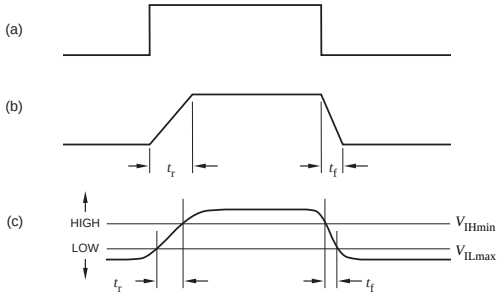
The voltage shift may not matter for analog applications (LEDs). But the output should not also be connected to inputs of CMOS gates.

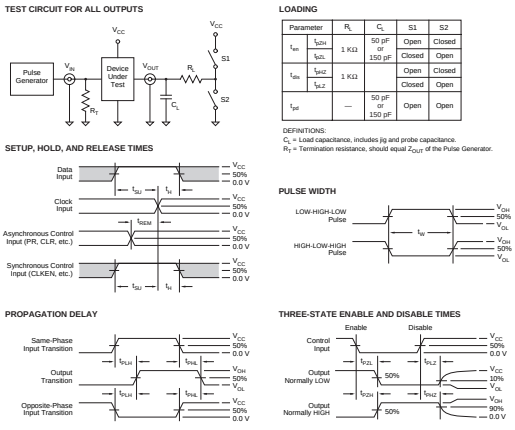
Intermediate input voltages (e.g., $2.5\,\mathrm{V}$) cause both transistors to turn on partially and steady state current to flow.

Unused inputs should be connected to some signal or voltage level.

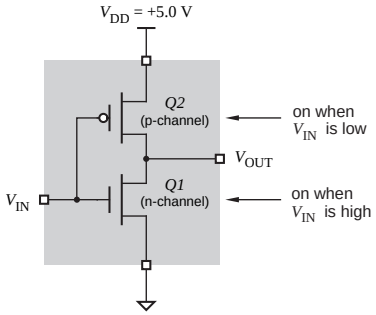


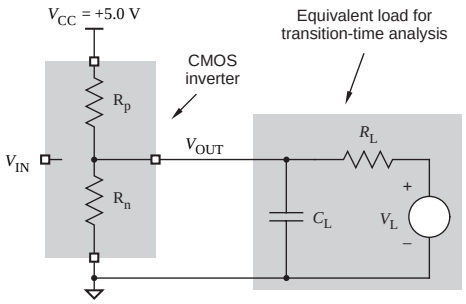
Timing diagrams

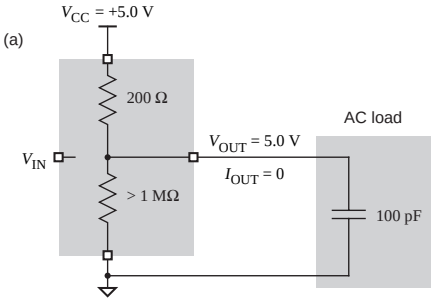


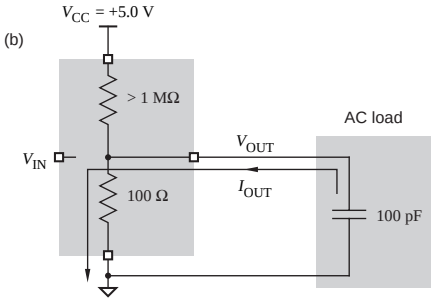


CMOS dynamic electrical behavior

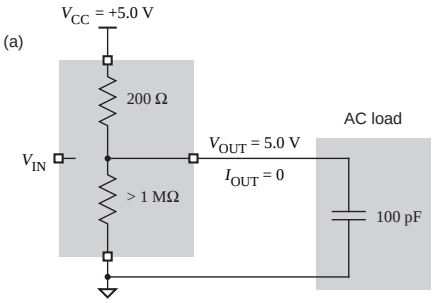


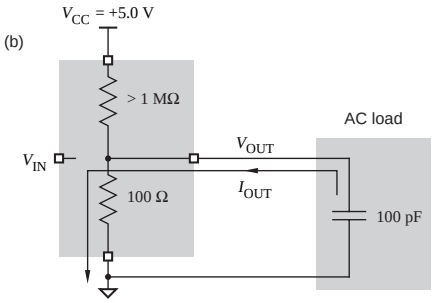




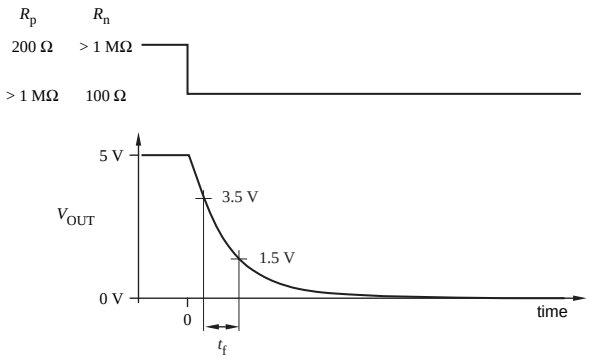


CMOS dynamic electrical behavior (2)

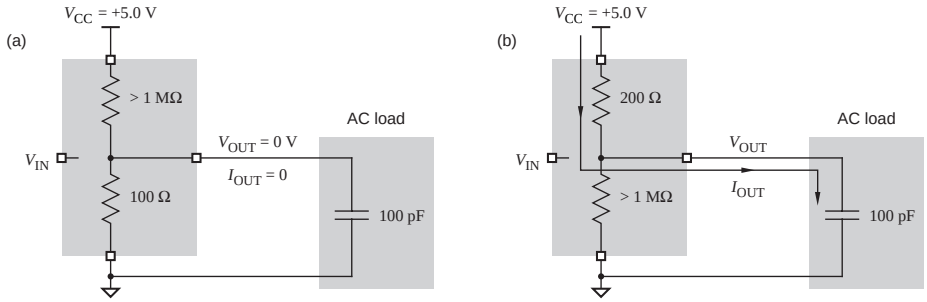




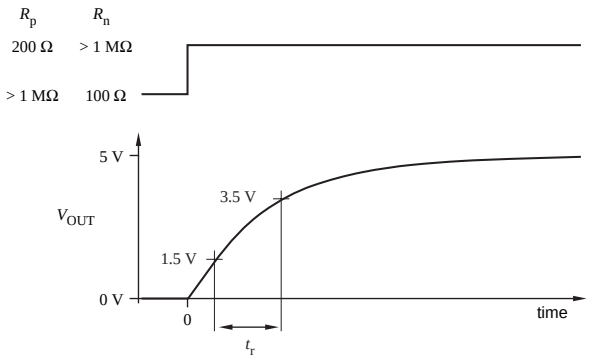
Fall time for high-to-low transition of CMOS output



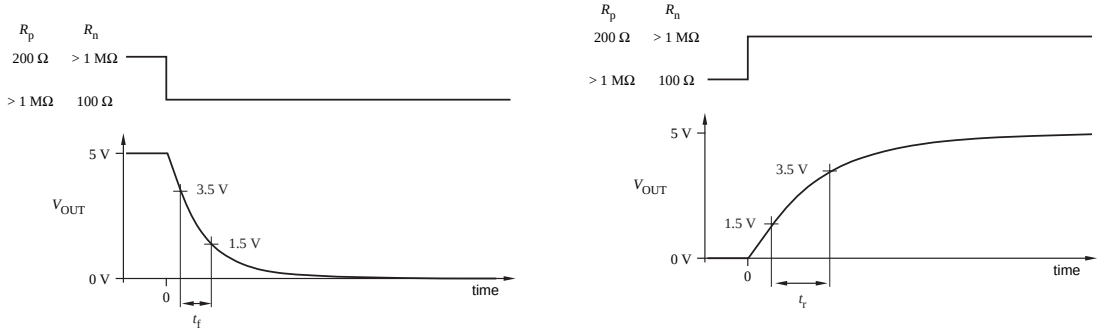
CMOS dynamic electrical behavior (3)

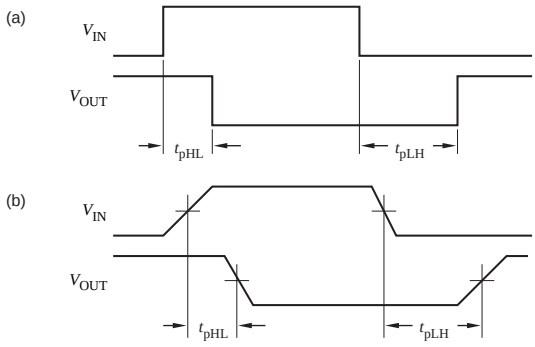


Fall time for low-to-high transition of CMOS output



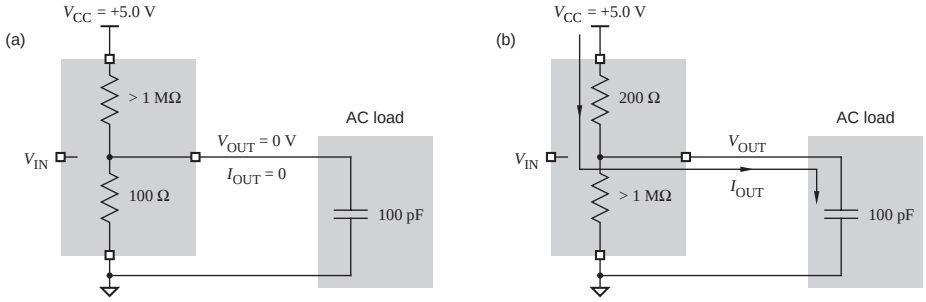
Propagation delays



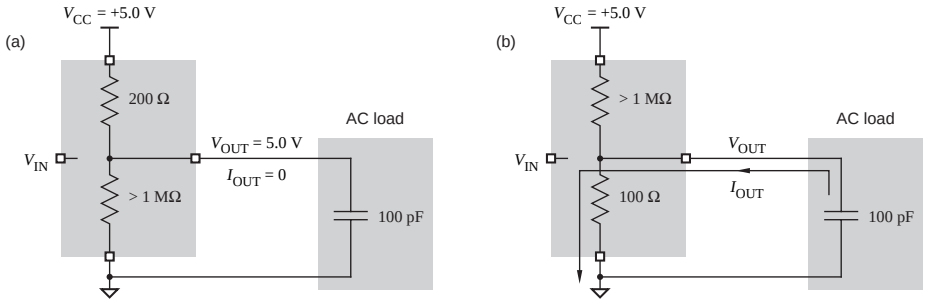


Power consumption

Current flows from power to ground through transistors, but may pause on capacitors (input gates of other CMOS devices).



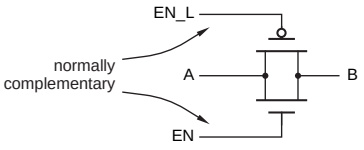
Power consumption (2)



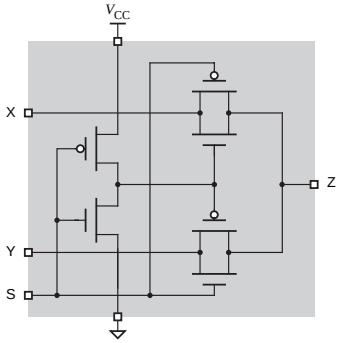
Power consumption formula: $P = C_{\mathrm{PD}} \cdot V_{\mathrm{DD}}^2 \cdot f$

C_{PD}	effective capacitance
V_{DD}	power-supply voltage
f	number of output transitions per second

Transmission gates

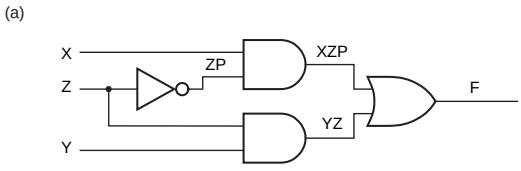


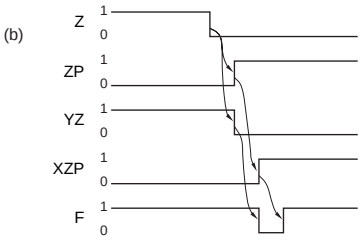
Multiplexers can be built using T-gates:



Transmission gates (2)

This circuit uses only 6T compared to 14T for the NAND-NAND circuit:





Warning: delays through transmission gates can add up.