EE 121
Digital Design Laboratory

November 7, 2002
Handout #25

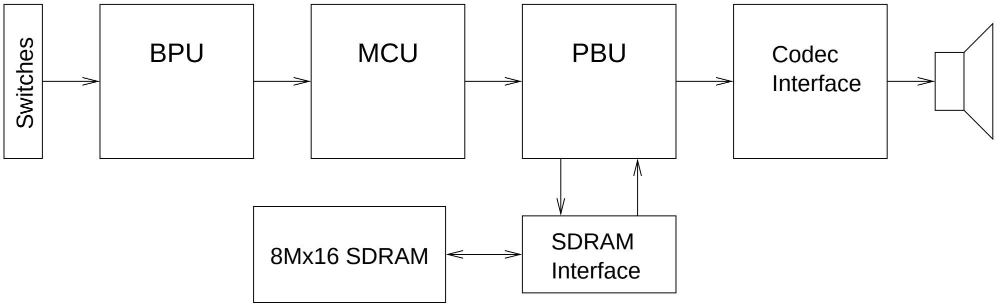
Laboratory Assignment #6

Digital Audio Player

Prelab due date: Tuesday, November 12, 5:00pm

Design and implement a digital audio player using the XESS XSA-100 Spartan-2 and XStend boards. The digital audio player will play samples stored in the 16MB SDRAM on the XSA-100 board. The SDRAM contains four tracks, each consisting of 64K 16-bit samples or about 8 seconds of audio. Your digital audio player will play the track selected by the user.

A block diagram and suggested decomposition of the audio player is shown below.



The chief components shown in the block diagram above are:

- Button Processor Unit (BPU)
- Master Control Unit (MCU)
- Playback Unit (PBU)
- Synchronous Dynamic Random Access Memory (SDRAM)
- AKM 4520 Audio Encoder/Decoder (CODEC)

These components are described in the following sections.

Button Processor Unit (BPU)

The BPU accepts inputs from four switches representing play forward, play reverse, stop, and track advance. These four switches can produce six different events; these events and the implications are:

- Stop pressed: Stop playing and reset to the beginning of track 1.
- Track pressed: Jump to the beginning of the next track and play.
- Play (forward or reverse) held < 0.5 seconds: Play in the specified direction at normal speed.

- Play (forward or reverse) held > 0.5 seconds: Play in the specified direction at twice normal speed.

A change in speed should continue playing from the same point at which the button press is received, i.e., no skipping within the track.

Master Control Unit (MCU)

The MCU interprets the output of the BPU and maintains state information about the digital audio player. In the MCU, the state information is decoded and passed on to the playback unit. The state of the MCU represents the current mode of the audio player (e.g., stopped or playing double-speed reverse). You should resolve the possibility of multiple simultaneous events by assigning a priority to each event.

Playback Unit (PBU)

The PBU accepts state information and generates addresses for the SDRAM. The highest two address bits encode the track number, and the low 16 address bits are sample numbers within each track. The sample rate is approximately 8 KHz. When the end of a track is reached, the track repeats.

Synchronous Dynamic Random Access Memory (SDRAM)

The digital audio player plays back sampled sounds stored in the XESS board SDRAM by counting through the SDRAM addresses. You will be provided with files containing sound data. The sound files will be downloaded to the SDRAM by dragging the sound file to the RAM area of XSLOAD when downloading the FPGA design.

The SDRAM acts as a lookup table; the SDRAM is not written to in this laboratory assignment. You provide an 18-bit address and raise the READ signal. (The RAM device requires 23 address bits; the high-order 5 bits are not used here and should be set to zero.)

The data is available to read when the DONE signal is high. This may not happen for 10 to 20 of the 25 MHz clock cycles. Your design needs to handle the variability in when data is available for reading. The delay has to do with the refreshing of dynamic RAM and will be discussed later in the term.

A starter SDRAM project will be provided with more information.

AKM 4520 Audio Encoder/Decoder (CODEC)

To produce the sound, the digital data stored in the SDRAM must be converted to an analog signal. The Asahi Kasei Microsystems 4520 coder/decoder (CODEC) on the XESS XStend board will perform this function. See the EE 121 WWW page for a sample codec application and documentation. You should take the codec schematic and use it in your design to output sound to the speakers.

LABORATORY REQUIREMENTS

A top-level schematic will be provided on the course WWW page that includes signal names and pin assignments. Please make sure that all signals defined in this file are still in your design.

For all your logic blocks, you can use any of the elements in the Foundation library (including CoreGen) but **you must not gate the clock**. This means that all state machines must be fully synchronous.

What to turn in for this week's prelab:

1. Complete Foundation Project with schematics of all logic blocks in your design (submitted electronically)
2. Test script demonstrating that your design works (submitted electronically)
3. A report file that specifies resources used in the FPGA for the design, i.e., the number of CLBs/IOBs/etc used. Look under the "Reports" in Xilinx foundation. Summarize and discuss the results in your `README` in one paragraph (submitted electronically)
4. Extract timing information for the design as demonstrated in lecture and submit the file. The "Analyze against Auto Generated Design constraints…" button in the Xilinx Timing Analyzer tool will provide the values needed. Summarize and discuss the results in your `README` in one paragraph (submitted electronically)
5. JPEG screen dump submitted electronically
6. `README` file (submitted electronically).

For this laboratory assignment, partners should work together and partition the work of designing the various components (PBU, MCU, PBU).

LABORATORY EXERCISE

During lab time, you will get a chance to compile your design, download it onto your Xilinx chip, and test it with real signals.

SUBMISSION

Submit this lab using the same instructions as for previous labs.

You must submit your project electronically, whether or not it works correctly, by 5:00pm on the due date or you will receive no credit.