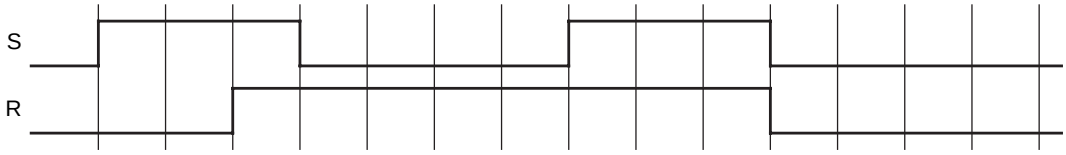
EE 121 November 7, 2002
Digital Design Laboratory Handout #24

Homework #3

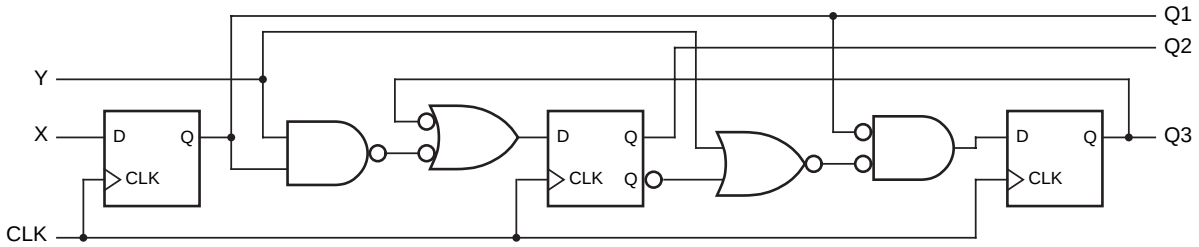
Due: Thursday, November 14

1. (*DDPP* 7.3) S-R *latch timing.* Sketch the outputs of an S-R latch of the type shown in Figure 7-5 for the input waveforms shown in Figure X7.3. Assume that input and output rise and fall times are zero, that the propagation delay of a NOR gate is 10 ns, and that each time division below is 10 ns. Although you may find the result unbelievable, this behaviour can actually occur in real devices whose transition times are short compared to their propagation delay.



2. (*DDPP* 7.5) J-K *vs.* T *flip-flops.* Show how to build a J-K flip-flop using a T flip-flop with enable and combinational logic.

3. (*DDPP* 7.16) *State machine analysis.* Analyze the clocked synchronous state machine in Figure X7.16. Write excitation equations, excitation/transition table, and state table (use state names A–H for Q2 Q1 Q0 = 000–111).



4. (*DDPP* 8.27) *Ripple counter.* Design a 4-bit ripple counter using four D flip-flops and no other components.

5. *Triangle wave counter.* Use a 74x169 up/down counter and additional combinational and sequential logic to build a free running counter that counts up and down repeatedly, cycling through the values $\ldots, 0, 1, 2, \ldots, 13, 14, 15, 14, 13, \ldots, 2, 1, 0, 1, 2, \ldots$ Important: do not use /RCO or any other output that might glitch as a clock to any sequential circuits.