EE 121 March 6, 2001
Digital Design Laboratory Handout #33

Midterm Examination #2

Open book, open notes. Time limit: 2 hours

Honor Code Acceptance: This examination has been written according to the spirit and principles of the Stanford Honor Code.

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Signature

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Print Name

Problem	Score
#1	/ 12
#2	/ 13
#3	/ 20
#4	/ 20
#5	/ 10
#6	/ 25
Total	/ 100

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1. (12 points) *Multiplication.* The unsigned product of 2-bit numbers $\mathsf{A}_1\mathsf{A}_0$ and $\mathsf{B}_1\mathsf{B}_0$ is a 4-bit result $\mathsf{Y}_3\mathsf{Y}_2\mathsf{Y}_1\mathsf{Y}_0$. For example,

$$11_2 \cdot 11_2 = 3_{10} \cdot 3_{10} = 9_{10} = 1001_2 \,.$$

Find efficient Boolean formulas for the product bits $\mathsf{Y}_3\mathsf{Y}_2\mathsf{Y}_1\mathsf{Y}_0$ as functions of the bits of the multiplier $\mathsf{A}_1\mathsf{A}_0$ and the multiplicand $\mathsf{B}_1\mathsf{B}_0$.

Y_0 = _____

Y_1 = _____

Y_2 = _____

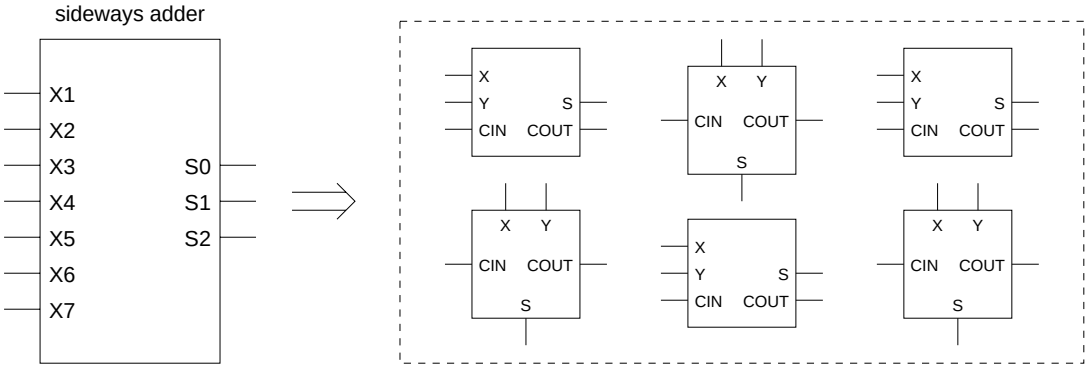
Y_3 = _____

Hint: the formulas for Y_0 and Y_3 are *very* simple. Remark: the best equations are *not* the minimal sums of products.

2. (13 points) *Sideways adder.* The *sideways sum* of a signal vector $(\mathsf{X}_1, \mathsf{X}_2, \ldots, \mathsf{X}_n)$ is the number of input signals that are true; that is,

$$\mathsf{S} = \sum_{k=1}^{n} \mathsf{X}_k \,.$$

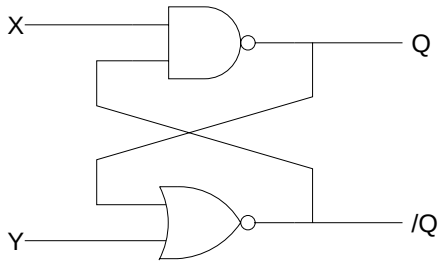
Since S has $n+1$ possible values, the sum requires a vector of $m = \lceil \log_2(n+1) \rceil$ bits. For $n = 7$, the sum is represented by $\lceil \log_2(7+1) \rceil = \lceil \log_2 8 \rceil = 3$ bits; that is, $\mathsf{S} = (\mathsf{S}_2, \mathsf{S}_1, \mathsf{S}_0)$.



Using only full adders, design a circuit that calculates the sideways sum $(\mathsf{S}_2, \mathsf{S}_1, \mathsf{S}_0)$ of $(\mathsf{X}_1, \mathsf{X}_2, \ldots, \mathsf{X}_7)$. You may use either of the two alternative logic symbol for the full adder. (Do not try to wire the full adders inside the box above.) Hint: six full adders are more than enough. Bonus points for minimum number of gates and smallest propagation delay.

3. (20 points) *Latches?*

   a. A committee of logic designers could not agree on whether to use NAND gates or NOR gates to build a set-reset latch. The compromise design is shown below.

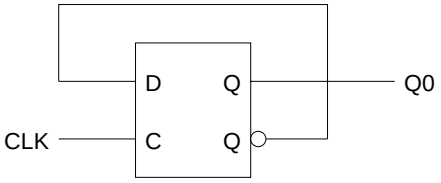


   Fill in the function table for this sequential circuit.

X	Y	Q	/Q
0	0		
0	1		
1	0		
1	1		

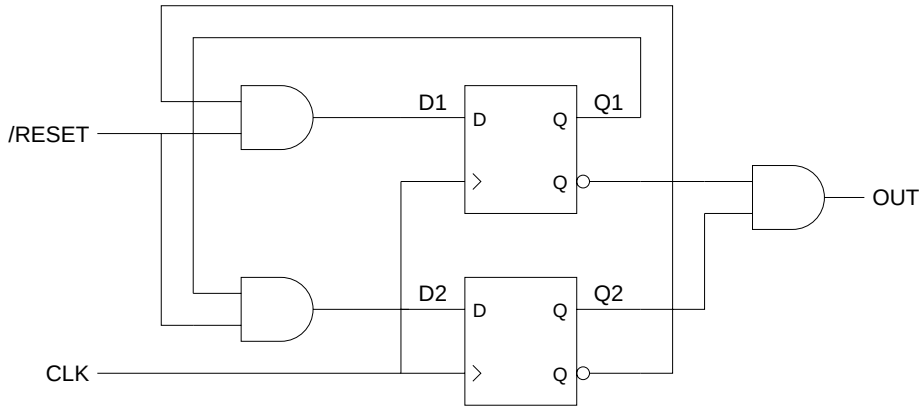
   Explain what is wrong with this "latch"?

   b. The feedback sequential circuit shown below is intended to change state with each clock pulse; in other words, it is supposed to be a "toggle latch."



   Explain why this sequential circuit does not work as intended. What actually happens?

4. (20 points) *State machine analysis.* Analyze the clocked synchronous state machine below.



a. Draw a state diagram for this state machine.

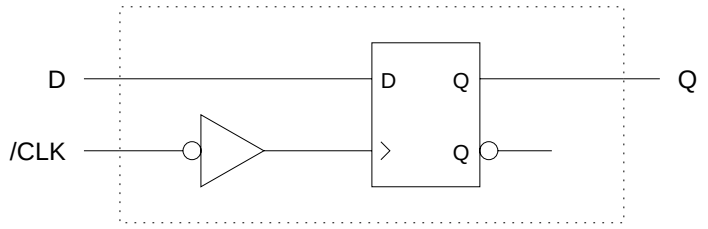
b. Is this machine a Mealy machine or a Moore machine?

Answer (circle one): Mealy Moore

c. Fill in the transition/output table for the above state machine.

	/RESET		
Q1 Q2	0	1	OUT
0 0			
0 1			
1 0			
1 1			
	Q1*Q2*		

5. (10 points) A negative edge-triggered D flip-flop can be built from a positive edge-triggered D flip-flop and an inverter, as shown below.



The propagation delays and timing parameters for the inverter and the D flip-flop are given in the following tables.

Inverter		
	min	max
t_{pLH}	5	7
t_{pHL}	3	5

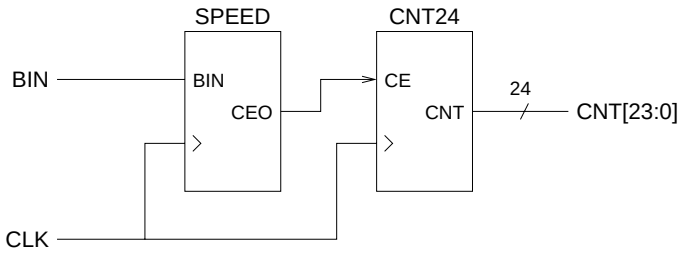
Flip-Flop	
t_{s}	6
t_{h}	2

Find the setup time t_{s} and the hold time t_{h} for this negative edge-triggered flip-flop.

Setup time t_{s} = _____

Hold time t_{h} = _____

6. (25 points) *Variable-speed counter.* The 24-bit binary counter shown below counts either at full speed or at half speed as determined by the speed-control state machine SPEED.



In half-speed mode, SPEED enables counting on every other clock, whereas in full-speed mode, the counter enable CE is always true. The speed is changed by the pushbutton input BIN; each positive pulse of BIN toggles the speed mode, from half to full or from full to half. This input is debounced, and its pulse width is a large number of clock cycles.

a. Draw the state diagram for the SPEED state machine.

b. For a state assignment of your choice, write the transition/output table.

c. For the state assignment of part b, write the transition and output equations.