EE 121 May 30, 2002
Digital Design Laboratory Handout #33

**Midterm Examination #2**

Open book, open notes. Time limit: 75 minutes

Honor Code Acceptance: This examination has been written according to the spirit and principles of the Stanford Honor Code.

_____
Signature

_____
Print Name

| Problem | Score |
|---|---|
| #1 | / 20 |
| #2 | / 20 |
| #3 | / 30 |
| #4 | / 30 |
| Total | / 100 |

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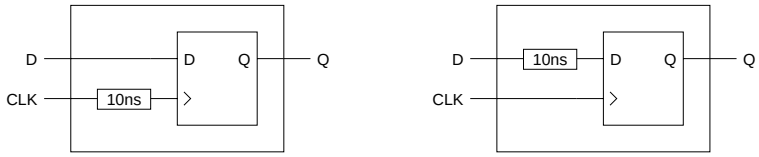
1. (20 points) *Setup and hold times.* The D flip-flops below have setup time $t_s = 18\,\text{ns}$ and hold time $t_h = 4\,\text{ns}$.

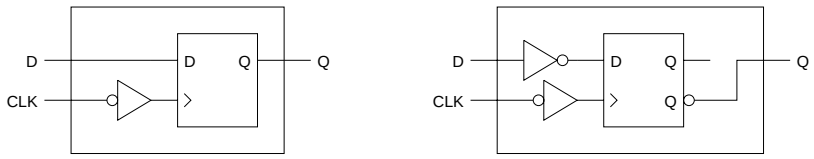



a. Suppose the clock is delayed by exactly 10 ns. (See the left device in the figure above.) What are the setup and hold times for this modified flip-flop?

Setup time: $t_s =$ _____ Hold time: $t_h =$ _____

b. Suppose the data input is delayed by exactly 10 ns. (See the right device in the figure above.) What are the setup and hold times for this modified flip-flop?

Setup time: $t_s =$ _____ Hold time: $t_h =$ _____




c. A negative-edge-triggered flip-flop can be built from a positive-edge-triggered flip-flop by inverting the clock input. (See the left device in the figure above.)

Propagation delays in nanoseconds for the inverter are given in the following table.

| | min | max |
|---|---|---|
| $t_{LH}$ | 12 | 22 |
| $t_{HL}$ | 8 | 16 |

Find the setup and hold times for the modified flip-flop.

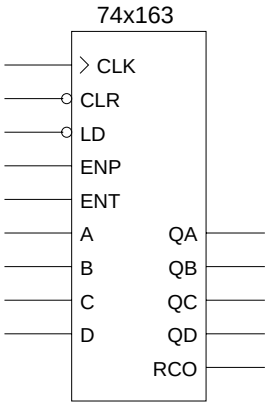
Setup time: $t_s =$ _____ Hold time: $t_h =$ _____

d. As you have discovered in parts (a) and (c), delaying the clock increases the hold time. To reduce the hold time, we might add delay to the data input, as shown in the right device in the figure above. (Note that the output of the modified flip-flop must now be taken from the internal flip-flop's complemented output.) Find the setup and hold times for this negative-edge-triggered flip-flop.

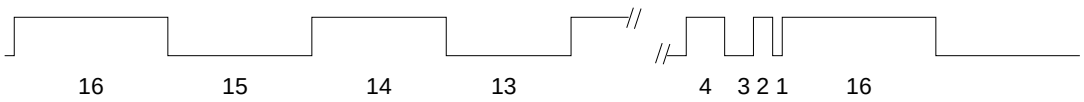
Setup time: $t_s =$ _____ Hold time: $t_h =$ _____

2. (20 points) *Fun with counters.*

   a. A *superstitious counter* is a free-running 4-bit counter that skips the value 13. Build a superstitious counter using one 74x163 4-bit counter and two 2-input gates.



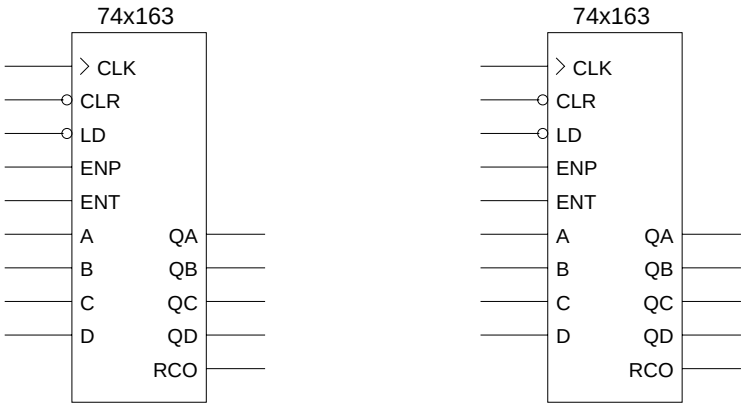

   b. The output of a *chirp counter* is the following waveform.




   The chirp output is high for 16 clocks, low for 15, high for 14, and so on until it is high of one clock duration. Then the cycle repeats. The overall period of this counter is

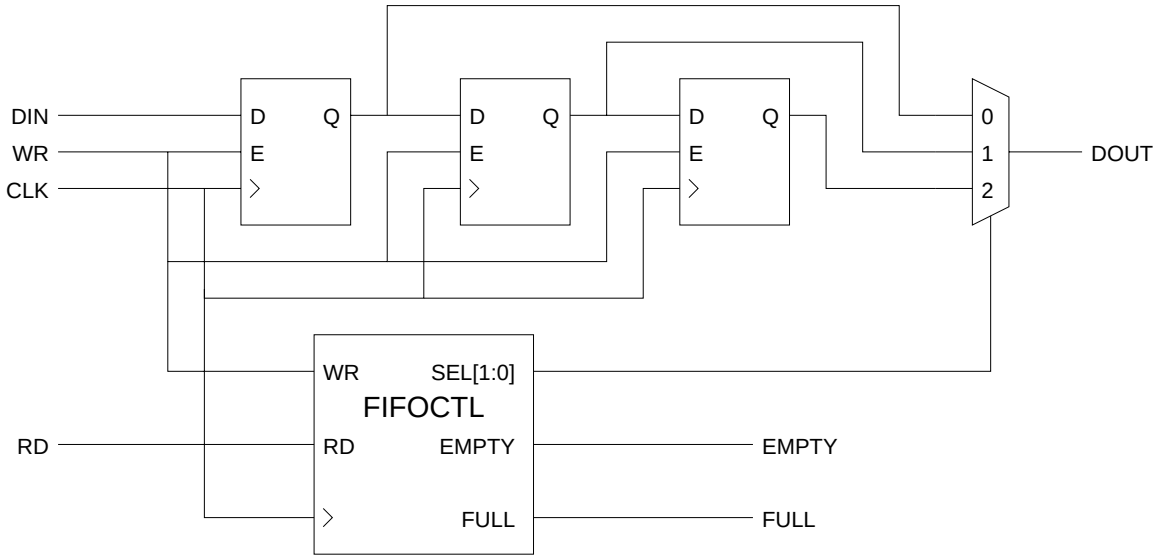
$$16 + 15 + \cdots + 2 + 1 = (17 \cdot 16)/2 = 136\,.$$

   Use two 4-bit counters and assorted gate(s) to build a chirp counter.



3. (30 points) *FIFO.* A 3-deep FIFO stores up to three words of data that are retrieved ("read") in a first-in first-out manner. The state of the FIFO control unit is the two-bit binary number in the range $\{0, \ldots, 3\}$ that tells how many words are stored in the FIFO.

   The FIFO state machine has two control inputs, RD ("read") and WR ("write"), and two outputs, FULL and EMPTY. The FIFO controller also has internal signals, SEL0 and SEL1, that select which stored data value to supply to the output.




   The control inputs are examined at each rising edge of the system clock. When WR alone is asserted, the FIFO state is incremented by 1, whereas when RD alone is asserted, the FIFO state is decremented by 1. If both RD and WR are asserted when the FIFO is nonempty, the FIFO state remains unchanged, since a new word is written into the FIFO while the oldest word is read and removed. Finally, when neither RD nor WR is active, the FIFO remains unchanged.

   The FIFO silently ignores attempts to write when it is full or to read when it is empty. The Moore outputs FULL and EMPTY report when the FIFO is full or empty, respectively.

*(Continued on next page)*

a. Fill in the following transition/output table for the FIFO state machine.

| Q1 Q0 | RD, WR | | | | FULL | EMPTY |
|---|---|---|---|---|---|---|
| | 00 | 01 | 10 | 11 | | |
| 0 0 | | | | | | |
| 0 1 | | | | | | |
| 1 0 | | | | | | |
| 1 1 | | | | | | |
| | Q1*,Q0* | | | | | |

b. Find *simplified* transition/output equations for the FIFO state machine.

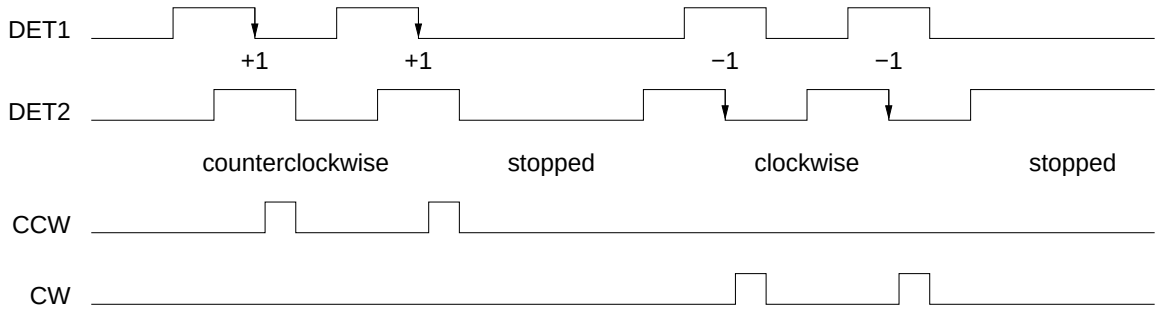
Q1* = _____

Q0* = _____

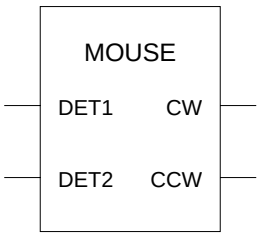
FULL = _____

EMPTY = _____

4. (30 points) *Mouse encoder.* The optical encoder wheel in a mechanical ball mouse produces detector pulses that indicate the speed and direction of motion.




Draw the state diagram of a clocked synchronous state machine whose inputs are the detector pulses and whose outputs are signals that can be used by an up/down counter.




This state machine has two Moore outputs, CW and CCW. CW should be active for one clock period when the encoder wheel has completed a clockwise step (indicated by the down arrows in the timing diagram), and CCW should be active for one clock period when the disk has completed a counterclockwise step.

Your state machine must accommodate input signals that are *not* debounced; you may assume that the output of each detector is stable before the other detector output changes.

This problem is open ended; there are quite a few situations to consider. More credit will be given for more complete solutions.

**Answer sheet for mouse encoder state diagram**