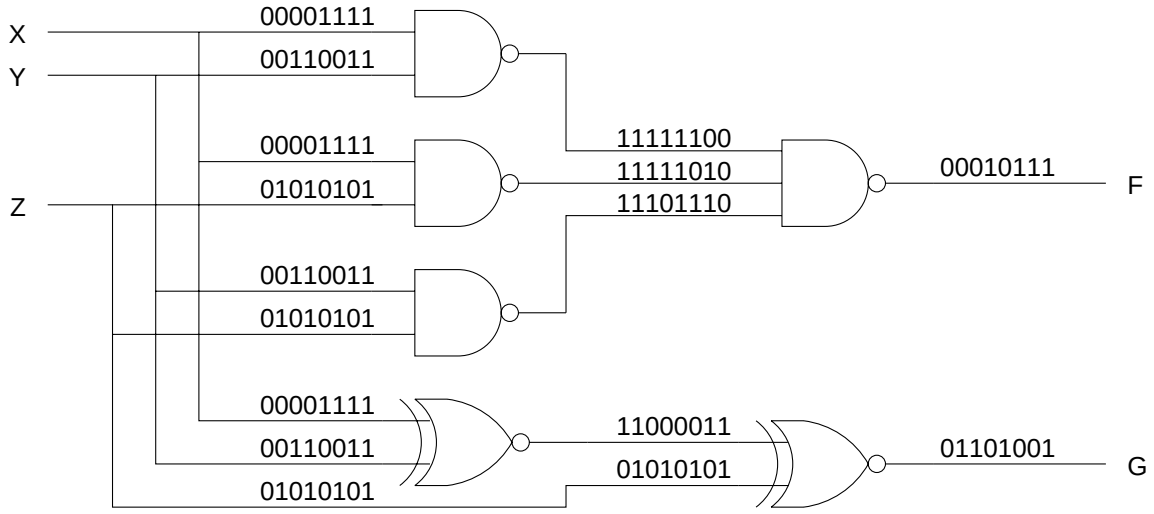
EE 121 February 8, 2001
Digital Design Laboratory Handout #19

Midterm Examination #1 Solutions

1. (30 points) *Combinational circuit analysis and timing.* The logic circuit below has three inputs, X, Y, and Z, and two outputs, F and G.



a. Find the minterm list and maxterm list representations for the outputs F and G.

Function	Minterm list	Maxterm list
F	$\Sigma_{XYZ}(3, 5, 6, 7)$	$\Pi_{XYZ}(0, 1, 2, 4)$
G	$\Sigma_{XYZ}(1, 2, 4, 7)$	$\Pi_{XYZ}(0, 3, 5, 6)$

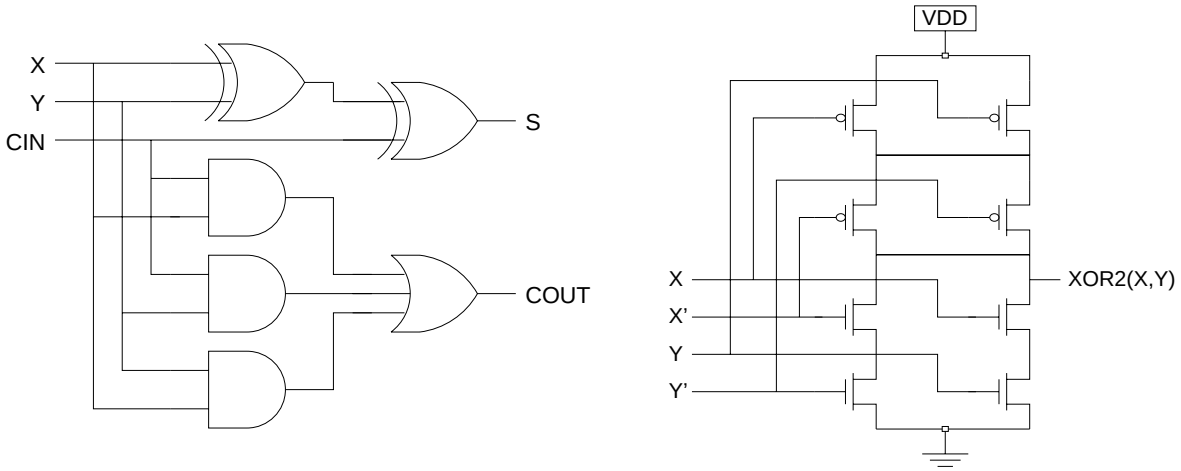
These functions are familiar. F is the majority function, while G is the exclusive-or of three inputs. In other words, the above circuit is an implementation of a full adder.

b. The propagation delays for the NAND gates in the above circuit are $t_{\text{pLH}} = 5$ ns and $t_{\text{pHL}} = 3$ ns. What are the worst case propagation delays from X to F? You may assume that wire delays are zero.

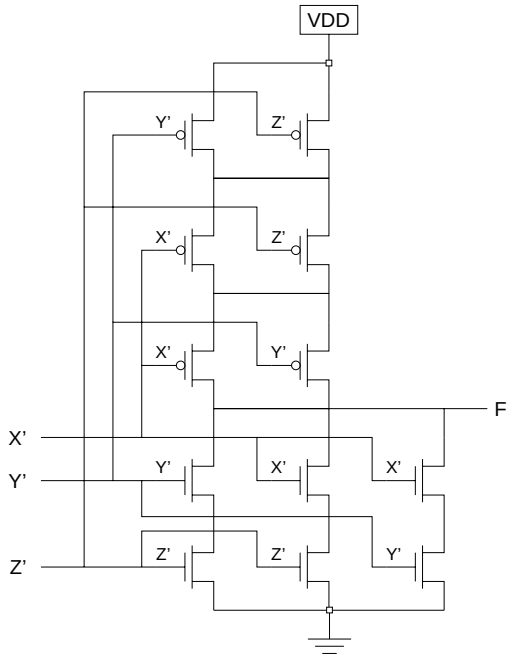
A change in X causes a low-to-high transition for F only when X goes high while exactly one of Y and Z is high. One of the two NAND gates with X as input goes low, causing the final NAND gate to go from low to high. The worst case propagation delay is $3+5 = 8$ ns. Similarly, when X goes from high to low, the worst case propagation delay is $5+3 = 8$ ns.

$t_{\text{pLH}}(\text{X}\rightarrow\text{F}) \;=\; 3+5 = 8$ ns $\qquad\qquad$ $t_{\text{pHL}}(\text{X}\rightarrow\text{F}) \;=\; 5+3 = 8$ ns

2. (20 points) *Full adder CMOS logic circuit.* A gate-level circuit diagram for a full adder and a CMOS logic circuit for an XOR gate are shown below. The XOR can be built with only 8 transistors, provided the complements of the inputs are available. (For this problem, it is *not* necessary to understand how the XOR circuit works.)

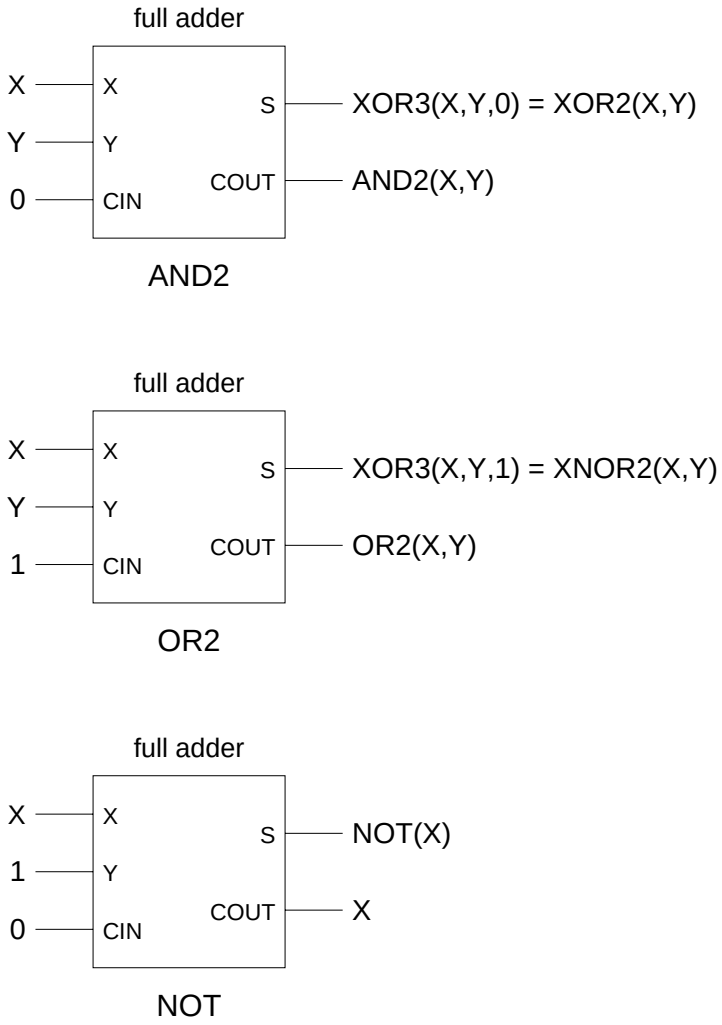


Since the complements of the inputs are needed for the XOR circuit, it makes sense to use them elsewhere in a CMOS logic circuit for a full adder. Design a CMOS logic circuit using 12 transistors (6 p-channel and 6 n-channel) that computes COUT from the complements X′, Y′, CIN′ of the input signals. Hint: majority$(\mathsf{X}, \mathsf{Y}, \mathsf{Z})$ = minority$(\mathsf{X}', \mathsf{Y}', \mathsf{Z}')$.



The output F is connected to ground through a series connection of two n-channel transistors if any two of X', Y', or Z' are true. Otherwise, if at least two of X, Y, or Z are true, F is connected to VDD through at least one path. Thus F is the majority function. It is easy to eliminate two transistors by merging the pairs of transistors with input X'.

3. (20 points) *Full adders are complete.* Full adders form a *complete* set of logic gates; that is, every Boolean function can be implemented using only full adders.



a. Wire each of the full adders above to produce the specified logic function (AND2, OR2, or NOT). In each case, only one output of the full adder is used. The full adder inputs may be connected to primary input signals or to constant values 0 or 1.

b. In each case, the "unused" output of the full adder is a Boolean function. Write next to that output pin the name or formula for this bonus output.