EE 121 May 2, 2002
Digital Design Laboratory Handout #20

**Midterm Examination #1**

Open book, open notes. Time limit: 75 minutes

1. (20 points) *CMOS logic circuit.* Draw a circuit diagram, function table, and logic symbol in the style of *DDPP* Figure 3-19 for a CMOS gate with two inputs, A and B, and an output Z, where Z = 0 if A = 1 and B = 0, and Z = 1 otherwise. Hint: Six transistors.

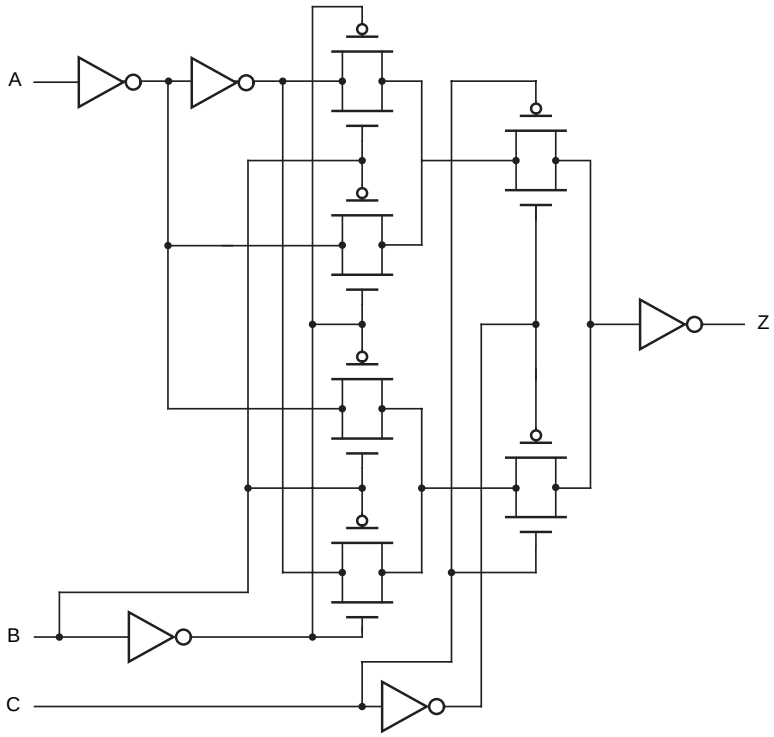
   Circuit diagram:

   Logic symbol:

   Function table:

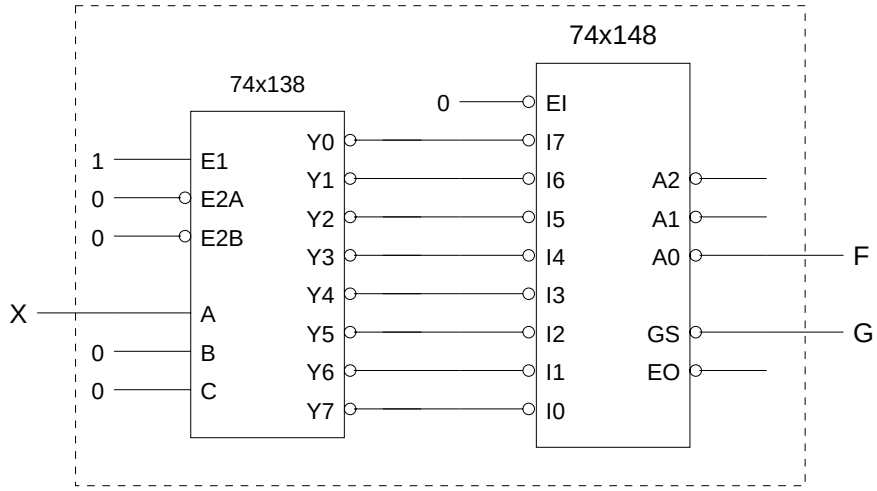
| A | B | *Q1* | *Q2* | *Q3* | *Q4* | *Q5* | *Q6* | Z |
|---|---|---|---|---|---|---|---|---|
| L | L | | | | | | | |
| L | H | | | | | | | |
| H | L | | | | | | | |
| H | H | | | | | | | |

2. (20 points) *CMOS circuit analysis.* Write the truth table and a logic diagram for the logic function performed by the following CMOS circuit.




| A | B | C | Z |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

3. (15 points) *MSI components.* A logic designer with time on his hands connected a 74x138 decoder and a 74x148 priority encoder as shown below.

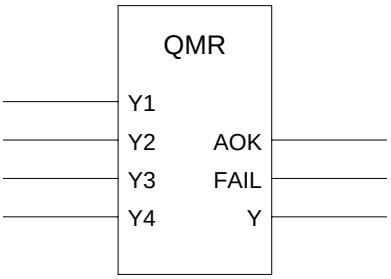



What logic functions are computed by F and G ?

F =

G =

4. (30 points) *Circuit synthesis.* A common method for building fault tolerance into digital systems is *triple modular redundancy* (TMR), in which a logic function is computed by three independent circuits and the final output is chosen by majority vote of the outputs of the three circuits. the final output is incorrect when two or three of the circuits are wrong. In this problem, we consider the even more reliable *quadruple modular redundancy*.




The QMR circuit shown in the figure above analyzes the outputs $\mathsf{Y1}, \mathsf{Y2}, \mathsf{Y3}, \mathsf{Y4}$ of four independent circuits for the same function.

- If all four values are the same, then AOK is true. (One use of AOK is to measure the failure rate of the circuits that compute $\mathsf{Y1}, \mathsf{Y2}, \mathsf{Y3}, \mathsf{Y4}$.)
- If there is no clear majority value for the four inputs—that is, two of $\mathsf{Y1}, \mathsf{Y2}, \mathsf{Y3}, \mathsf{Y4}$ are 0 and two are 1—then FAIL is true, which indicates that QMR cannot make a decision.
- When there is no failure, the output Y is the majority vote of the inputs $\mathsf{Y1}, \mathsf{Y2}, \mathsf{Y3}, \mathsf{Y4}$.

Write optimized Boolean equations (minimal sums of products) for each of the outputs of the QMR circuit.

AOK =

FAIL =

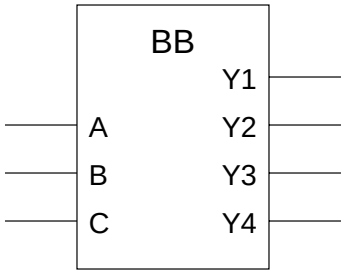
Y =

Your equations for Y should be simplified by using the fact that the value of Y does not matter when FAIL is true.

5. (20 points) XOR *trees.* The combinational logic propagation delays for the component shown below are different for the four outputs, as shown in the following table.

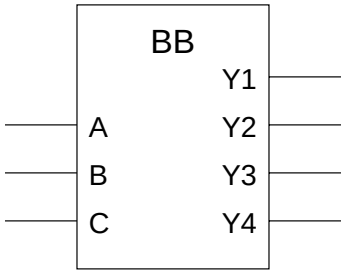
| From (input) | To (output) | Max |
|---|---|---|
| Any | Y1 | 10 ns |
| Any | Y2 | 20 ns |
| Any | Y3 | 30 ns |
| Any | Y4 | 40 ns |

a. Suppose that the propagation delay of an XOR gate is 10 ns. Connect three 2-input XOR gates to compute Y = XOR(Y1, Y2, Y3, Y4) so that the propagation delay from inputs A, B, C to output Y is minimized. What is this minimum propagation delay?




Propagation delay (XOR delay 10 ns): _____

b. Suppose that the propagation delay of an XOR gate is 30 ns. Connect three 2-input XOR gates to compute Y = XOR(Y1, Y2, Y3, Y4) so that the propagation delay from inputs A, B, C to output Y is minimized. What is this minimum propagation delay?




Propagation delay (XOR delay 30 ns): _____