Design and optimization of LC oscillators

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Abstract

We present a method for optimizing and automating component and transistor sizing for CMOS LC oscillators. We observe that the performance measures can be formulated as *posynomial* functions of the design variables. As a result, the LC oscillator design problems can be posed as a *geometric program*, a special type of optimization problem for which very efficient *global* optimization methods have recently been developed. The synthesis method is therefore fast, and determines the globally optimal design; in particular the final solution is completely independent of the starting point (which can even be infeasible), and infeasible specifications are unambiguously detected. We can rapidly compute globally optimal trade-off curves between competing objectives such as phase noise and power.

1 Introduction

LC oscillators are commonly used in CMOS radio-frequency integrated circuits (RF-ICs) because of their good phase noise characteristics and their ease of implementation [1, 2, 3, 4, 5]. However, no systematic design methodology exists to account for the many specifications (phase noise, power dissipation, voltage swing, tuning range ...). Typical design strategies have tried to achieve a low phase noise by using the largest possible inductance value [3], or by using inductors with the lowest possible series resistance [4]. However, an optimal design requires the simultaneous consideration of both active and passive devices.

In this paper, we propose a new method for the design of LC oscillators. We illustrate our technique for the specific architecture of Figure 1. The method is easily extensible to other LC oscillator architectures. We formulate the design problem as a special type of optimization problem, called geometric programming (GP). We provide an overview GP in §2 and then outline the design variables in §3. In §4, we obtain the equivalent circuit model for the LC oscillator using the inductor model presented in [6] and simple transistor models. In §5, we use these models and the phase noise model of [5] to show how the design specifications can be posed in a way suitable for geometric programming.

This geometric program formulation allows us to obtain globally optimal designs very efficiently, thereby permitting the designer to spend more time exploring design trade-offs rather than sizing inductors and devices. We illustrate our method with design examples in §6 and optimal performance tradeoff curves in §7.

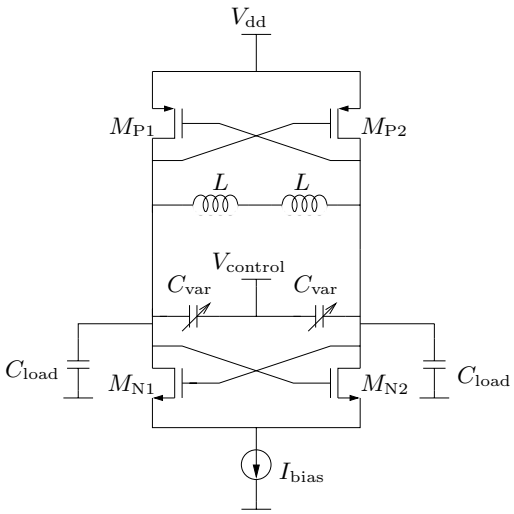

Figure 1: Complementary LC oscillator.

2 Geometric Programming

Let f be a real-valued function of n real, positive variables $x_1, \ldots, x_n$. It is called a *posynomial* function if it has the form

$$f(x_1, \ldots, x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_n^{\alpha_{nk}},$$

where $c_j \geq 0$ and $\alpha_{ij} \in \mathbf{R}$. When $t = 1$, f is called a *monomial* function. A *geometric program* (see [7]) has the form

$$\begin{array}{ll} \text{minimize} & f_0(x) \\ \text{subject to} & f_i(x) \leq 1, \quad i = 1, 2, \ldots, m, \\ & g_i(x) = 1, \quad i = 1, 2, \ldots, p, \\ & x_i > 0, \quad i = 1, 2, \ldots, n, \end{array} \tag{1}$$

where f_i are posynomial functions and g_i are monomial functions.

The most important feature of geometric programs is that they can be *globally* solved with great efficiency, with no initial point needed, using newly developed interior-point methods [8, 9, 10]. To carry out the designs described in this paper we implemented in MATLAB a very simple (primal barrier) method for solving the convex form of a GP [10]. Despite the simplicity of the method, and the inefficiency of our implementation, all the design problems in this paper were solved under one second on a personal computer.

3 Design variables

To design the oscillator we specify the following twelve variables:

- Spiral inductor: number of turns n, turn width w, turn spacing s and outer diameter $d_{\rm out}$.

- Transistors: width ($W_{\rm n}$ and $W_{\rm p}$) and length ($L_{\rm n}$ and $L_{\rm p}$).
- Varactor: maximum value $C_{\rm v,max}$ and minimum value $C_{\rm v,min}$.
- Load capacitance: $C_{\rm load}$.
- Bias current: $I_{\rm bias}$. Since the thermal noise of the tail current source in the vicinity of the frequency of oscillation does not affect the phase noise of the oscillator due to its differential operation [5], we use $I_{\rm bias}$ as a design parameter rather than the bias transistor dimensions.

4 Model for the LC oscillator

4.1 Inductor model

In this paper, we consider planar spiral inductors. One can easily extend the method to other inductors such as bond wires [1], auto-transformers [3] and non-standard spiral inductors [2].

A spiral inductor is characterized by the number of turns n, the turn width w, the turn spacing s, and the outer diameter $d_{\rm out}$. The inductor can be implemented with or without a patterned ground shield (PGS) [11] (a grounded polysilicon shield broken regularly in the direction perpendicular to the inductor current flow).

Figure 2 shows a commonly used circuit model for the inductor (with or without PGS) (see [6]). This model is accurate for lightly doped substrates as long as the assumption of a lumped model is valid. In [12], it is shown that the inductor circuit element values are posynomial functions of the design variables (n, $d_{\rm out}$, w and s). The inductance L can be modeled by a monomial function of the design variables with typical errors of only 3% (see [13]).

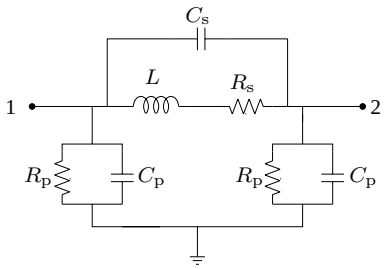

Figure 2: Simplified inductor model.

4.2 Varactor model

There are several varactor options for frequency tuning [14] such as junction diodes, MOS capacitors and accumulation mode capacitors. In this paper, we use a generic varactor model although models specific to a particular implementation can also be used. The varactor capacitance ranges from some minimum value $C_{\rm v,min}$ to some maximum value $C_{\rm v,max}$. The ratio $C_{\rm v,max}/C_{\rm v,min}$ is limited due to physical limitations of the varactor. The varactor quality factor $Q_{\rm v}$ depends on the frequency of operation. For simplicity, we assume a constant quality factor value equal to its minimum value across the tuning range. We model the varactor as an ideal capacitor in series with a resistor $R_{\rm v} = Q_{\rm v}/\left(C_{\rm v}\omega\right)$. We will see that this simplification is not critical since the varactor contributes little to the total oscillator phase noise (see §6).

4.3 Transistor model

We now describe an analytical model for short-channel devices. More accurate models for transistors that are still compatible for geometric programming are available [15].

- **Transconductance g_m:** A simple model for the transconductance of short-channel devices is [16],

$$g_{\rm m} = \mu C_{\rm ox} W E_{\rm sat}/2, \tag{2}$$

where μ is the mobility of the carriers in the channel, $C_{\rm ox}$ is the oxide capacitance, W is the transistor width, and $E_{\rm sat}$ is the field at which the carrier velocity reaches half its saturation velocity.

- **Output conductance g_d:** We use a simple monomial model for the short-channel transistor output conductance that was used in [15],

$$g_{\rm d} = \lambda I^{0.6} L^{-1} W^{0.4}, \tag{3}$$

where λ is a fitting parameter, I is the transistor drain current and L is the transistor channel length.

- **Capacitances:** We model the gate-to-drain ($C_{\rm gd}$), the drain-to-bulk ($C_{\rm db}$) and the gate-to-source ($C_{\rm gs}$) capacitances with posynomial expressions in the transistor width and length (see [16, 15]).

4.4 Tank model

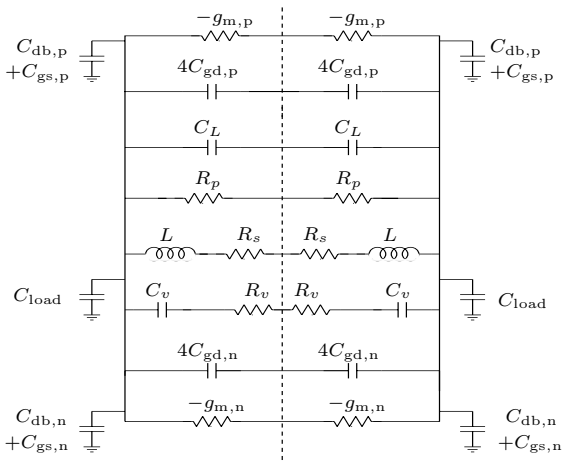

Figure 3: Complementary LC oscillator.

We model the tank with the equivalent small signal differential mode circuit shown in Figure 3, where the dashed lined is an effective AC ground for differential operation. We now define:

- **Tank inductance ($L_{\rm tank}$)**is given by the monomial,

$$L_{\rm tank} = 2L. \tag{4}$$

- **Tank capacitance ($C_{\rm tank}$)**is given by,

$$\begin{aligned} C_{\rm tank} = \; & \tfrac{1}{2}(4C_{\rm gd,n} + C_{\rm gs,n} + C_{\rm db,n} + 4C_{\rm gd,p} \\ & + C_{\rm gs,p} + C_{\rm db,p} + C_L + C_v), \end{aligned} \tag{5}$$

which is a posynomial function of the design variables since it is a sum of posynomial functions.

- **Tank load conductance ($g_{\rm tank}$)** is given by,

$$g_{\rm tank} = \left(g_{\rm d,n} + g_{\rm d,p} + g_v + g_L\right)/2, \tag{6}$$

where g_v, the effective parallel varactor conductance, and g_L, the effective parallel inductor conductance, are given by the posynomial expressions (see [12]),

$$g_v = \frac{C_{\rm var}\omega}{Q_v}, \qquad g_L = \frac{1}{R_{\rm p}} + \frac{1}{\left(L\omega\right)^2/R_{\rm s}}.$$

Since $g_{\mathrm{d,n}}$ and $g_{\mathrm{d,p}}$ are also given by posynomial functions of the design variables, expression (6) for g_{tank} is a posynomial function of the design variables.

- **Tank effective negative conductance ($g_{\mathbf{neg,tank}}$)** is determined by the transconductance of the cross-coupled transistor pairs. To improve the $1/f^3$ corner of the phase noise it is convenient to have a symmetric tank ($g_{m,n} = g_{m,p}$) [5]. For symmetric tanks, $g_{\mathrm{neg,tank}}$ is given by the monomial expression,

$$g_{\mathrm{neg,tank}} = -(g_{\mathrm{m,n}} + g_{\mathrm{m,p}})/2 = -g_{\mathrm{m,n}}. \tag{7}$$

5 Design specifications

We now show that the design specifications for the LC oscillator can be expressed as either monomial equality constraints, or posynomial inequality constraints, and therefore can be handled by GP.

Quiescent power

The quiescent power is given by the product of the supply voltage V_{dd} and the bias current I_{bias},

$$P = I_{\mathrm{bias}} V_{\mathrm{dd}}. \tag{8}$$

Since equation (8) is monomial, we can bound the maximum quiescent power with a monomial constraint ($P \leq P_{\max}$).

Differential voltage amplitude

The amplitude of the differential voltage across the tank is determined by whether the oscillator is operating in current limited mode or in voltage limited mode. It can be expressed as,

$$V_{\mathrm{amp}} = \min\{I_{\mathrm{bias}}/g_{\mathrm{tank}}, V_{\mathrm{dd}}\}. \tag{9}$$

We can impose a minimum swing ($V_{\mathrm{amp}} \geq V_{\mathrm{amp,min}}$) with the two monomial constraints,

$$V_{\mathrm{amp,min}} \leq V_{\mathrm{dd}} \qquad V_{\mathrm{amp,min}} \leq I_{\mathrm{bias}} R_{\mathrm{tank}}. \tag{10}$$

Phase noise model

In the $1/f^2$ region of the phase noise spectrum, the single sideband phase noise at an offset frequency (f_{off}) is given by [5]

$$\mathcal{L}(f_{\mathrm{off}}) = \frac{\Gamma_{\mathrm{rms}}^2}{8\pi^2 f_{\mathrm{off}}^2} \cdot \frac{\sum \overline{i_n^2}/\Delta f}{q_{\max}^2}, \tag{11}$$

where

- $\Gamma_{\mathrm{rms}} \approx 1/2$ for differential noise sources.
- $q_{\max}$ is the total charge swing of the tank and is given by the monomial expression,

$$q_{\max} = C_{\mathrm{tank}} V_{\mathrm{amp}} = \frac{V_{\mathrm{sw}}}{L_{\mathrm{tank}} \omega_{\mathrm{res}}^2}. \tag{12}$$

- $\sum \overline{i_n^2}/\Delta f$ is the sum of the current noise densities of the differential equivalent of individual noise sources: the transistor channel thermal noise ($\overline{i_{M,\mathrm{dT}}^2}/\Delta f$), the transistor gate noise ($\overline{i_{M,\mathrm{gT}}^2}/\Delta f$), the inductor thermal noise ($\overline{i_{RL}^2}/\Delta f$) and the varactor thermal noise ($\overline{i_{CV}^2}/\Delta f$), as depicted in Figure 4.

— Transistor channel thermal noise. In [5], it is shown that the total differential thermal current noise density due to the active devices is given by the posynomial expression,

$$\frac{\overline{i_{M,\mathrm{dT}}^2}}{\Delta f} = \frac{1}{2}\left(\frac{\overline{i_{M,\mathrm{dn}}^2}}{\Delta f} + \frac{\overline{i_{M,\mathrm{dp}}^2}}{\Delta f}\right), \tag{13}$$

where for short-channel devices,

$$\frac{\overline{i_{M,\mathrm{d}}^2}}{\Delta f} = \frac{4kT\gamma I_{\mathrm{bias}}}{E_{\mathrm{sat}} L}, \tag{14}$$

where k is Boltzman constant, T is the temperature in Kelvin and $\gamma \approx 2$ for short channel transistors. This simple model agrees well with measurements [5].

— Transistor gate noise. Since the gate noise sources are in parallel with the drain noise sources, they add in the same way [5]. Therefore, the total differential transistor gate current noise density is given by the posynomial expression,

$$\frac{\overline{i_{M,\mathrm{gT}}^2}}{\Delta f} = \frac{1}{2}\left(\frac{\overline{i_{M,\mathrm{gn}}^2}}{\Delta f} + \frac{\overline{i_{M,\mathrm{gp}}^2}}{\Delta f}\right), \tag{15}$$

where for short-channel devices,

$$\frac{\overline{i_{M,\mathrm{g}}^2}}{\Delta f} = \frac{4kT\delta\omega^2 C_{\mathrm{gs}}^2 E_{\mathrm{sat}} L}{5 I_{\mathrm{bias}}}, \tag{16}$$

where the parameter δ takes a value close to twice γ (see [16]) and C_{gs} is the gate to source capacitance. Since C_{gs} is given by a posynomial expression, equation (16) is also posynomial.

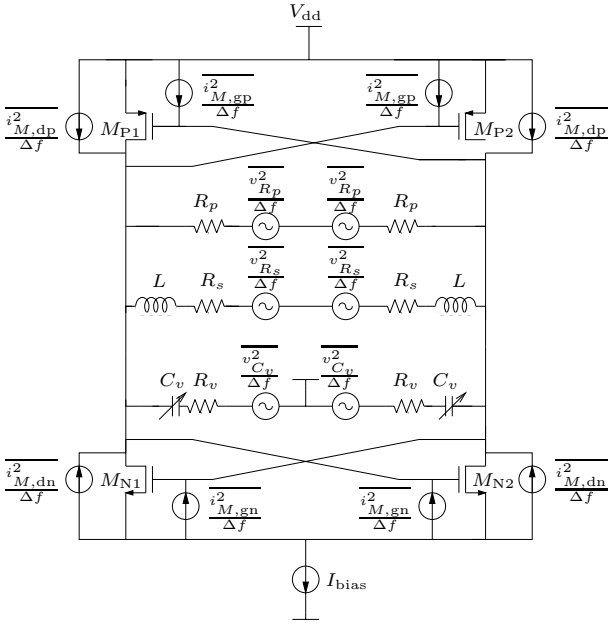

Figure 4: Noise sources in the LC oscillator.

—Inductor noise. There are two noise sources from the inductors: the ohmic losses in the winding and the losses in the substrate,

$$\frac{\overline{i_{RL}^2}}{\Delta f} = 2 \cdot \frac{4kT}{R_{\mathrm{L,p}}} \approx 8kT\left[\frac{1}{R_{\mathrm{p}}} + \frac{1}{(L\omega)^2/R_{\mathrm{s}}}\right]. \tag{17}$$

Since $R_{\rm p}$, L and $R_{\rm s}$ are given by monomial expressions (see [12]), equation (17) is a posynomial function of the design variables.

—Varactor noise. The varactor noise can be modeled with the monomial expression,

$$\frac{\overline{i_{CV}^2}}{\Delta f} = 2 \cdot \frac{4kT}{R_{\rm v,p}} \approx \frac{8kTC_{\rm v}\omega}{Q_{\rm v}}, \tag{18}$$

where $R_{\rm v,p}$ is the equivalent varactor parallel resistance.

Since $\Gamma_{\rm rms}$ is a constant, $q_{\max}$ is monomial in the design variables and the noise sources $\overline{i_n^2}/\Delta f$ are posynomial in the design variables, expression (11) is a posynomial equation of the design variables. Therefore, we can minimize the phase noise at a given frequency. To guarantee a minimum phase noise over the entire tuning range, we can impose the constraint ($\mathcal{L}(f_{\rm off}) \leq \mathcal{L}_{\max}(f_{\rm off})$) over several frequencies within the tuning range.

Resonance frequency

We can impose a constraint on the maximum resonance frequency $\omega_{\rm res,max}$. This constraint together with a constraint on the tuning range is equivalent to specifying a center resonance frequency. The maximum tank resonance frequency is given by the posynomial expression:

$$\omega_{\rm res,max} = \frac{1}{L_{\rm tank}C_{\rm tank,min}}. \tag{19}$$

We can therefore impose a minimum required $\omega_{\rm res,max}$ with the posynomial constraint $\omega_{\rm res,max} \geq \omega_{\rm res,max,req}$. This constraint is always active (*i.e.*, it is practically an equality). If it were not active the inductor could contribute additional capacitance to the tank, which would translate into a higher Q_L.

Tuning range

The tuning range is specified with two constraints

$$L_{\rm tank}C_{\rm tank,min} \leq 1/\omega_{\max}^2 \tag{20}$$

$$L_{\rm tank}C_{\rm tank,max} \geq 1/\omega_{\min}^2. \tag{21}$$

Constraint (21) is not posynomial and cannot be handled directly by GP. Since constraint (20) is always tight at the optimum, we can handle constraint (21) indirectly. We rewrite constraint (21) as,

$$\omega_{\min}^2 C_{\rm tank,max} \geq \omega_{\max}^2 C_{\rm tank,min}.$$

Now we let $r = \omega_{\rm res,max}^2/\omega_{\rm res,min}^2$, and obtain

$$(r-1)\frac{C_{\rm tank,min}}{C_{v,\max}} + r\frac{C_{v,\min}}{C_{v,\max}} \leq 1. \tag{22}$$

Thus, we can substitute (21) by the posynomial constraint (22).

Inductor constraints

It is shown in [12] that many inductor specifications have the form of posynomial inequalities. For example, specifications on minimum and maximum inductance, on maximum area, on minimum turn spacing and width are monomial while specifications on minimum quality factor and minimum self-resonance frequency are posynomial.

Geometry constraints

We can require that the width and length of the devices be constrained within some range using monomial constraints,

$$W_{\min} \leq W \leq W_{\max} \qquad L_{\min} \leq L \leq L_{\max}. \tag{23}$$

We can also limit the inductor area by imposing the monomial constraint $d_{\rm out}^2 \leq A_{\max}$.

Loop gain

For a complementary LC oscillator, the loop gain condition is

$$\left(g_{m,n} + g_{m,p}\right)/2 \geq \alpha_g g_{\rm tank},$$

where α_g is the excess gain and it is typically $\approx 2-3$. Since we have $g_{m,n} = g_{m,p}$ the loop gain condition is given by a posynomial constraint,

$$g_{m,n} \geq \alpha_g g_{\rm tank}.$$

Varactor tuning range

Although the absolute value of the varactor capacitance is typically not limited, the maximum tuning ratio $\beta_v = C_{\rm v,max}/C_{\rm v,min}$ is limited. We impose a maximum β_v with the monomial constraint $C_{\rm v,max} \leq \beta_v C_{\rm v,min}$.

6 Design examples

In this section, we show two oscillator designs. The LC oscillators are designed in a standard 0.35μm five metal layer 2.5V CMOS process.

Constraint	Specification	Achieved
Phase Noise 600kHz	minimize	-124.2dBc/Hz
$\omega_{\rm res}$	1.8GHz	1.8GHz
$C_{\rm load}$	$\geq$ 0.2nF	0.83nF
$I_{\rm tail}$	$\leq$ 5mA	5mA
$V_{\rm sw}$	$\geq$ 2V	2.5V
Tuning range	$\geq 10\%$	10%
$d_{\rm out}$	$\leq 300\mu$m	300μm
Excess loop gain α_g	≥ 3	3

Table 1: Specifications for example 1.

The objective in the first example is to minimize phase noise in an LC oscillator built using spiral inductors with PGS. The desired and achieved specifications are shown in Table 1. We note that many of the constraints are tight, *i.e.*, power, voltage swing, tuning range and area are all set to the limit specified. Table 2 shows the optimal oscillator design obtained. It is important to note that significant phase noise is contributed by both the transistors ($\approx 52\%$) and the inductors ($\approx 44\%$). This shows that a design solely based on maximizing the inductor or its quality factor will not be optimum.

In the second design example we limit $I_{\rm bias}$ to only 1.6mA. Table 3 shows the desired and achieved specifications. The differential swing voltage constraint is now tight. In table 4 we show the optimal design for the second example. The phase noise is around 7dB worse than in the first example and the relative contributions from the inductor and the transistors are $\approx 50\%$ and $\approx 46\%$, respectively.

This result is consistent with our intuition: increasing $I_{\rm bias}$ results in significant improvements in phase noise only if the oscillator operates in current limited mode. We cannot achieve a significant increase in the charge swing, $q_{\max}$, in the voltage limited mode. Therefore, if the available power is low, it is necessary to to operate in deep current limited regime. This corresponds to smaller average transistor currents which results in smaller noise current density. Optimization of the inductor Q is more helpful in this case.

Inductor	
L	3.9nH
n	4
d_{out}	300μm
w	23.2μm
s	1.8μm
R_s	6.5Ω
C_L	0.3pF
$R_{L,p}$	332Ω
Varactor	
$C_{\text{v,max}}$	0.81pF
$C_{\text{v,min}}$	0.41pF
$R_{v,p}$	$4.2\text{k}\Omega$

Transistors	
W_n/L_n	$17.0/0.35\mu$m
W_p/L_p	$52.7/0.35\mu$m
C_{NMOS}	0.07pF
C_{PMOS}	0.21pF
g_{m}	2mS
$1/g_{\text{ds,n}}$	$5.5\text{k}\Omega$
$1/g_{\text{ds,p}}$	$1.7\text{k}\Omega$
Tank	
R_{tank}	500Ω
C_{tank}	1.1pF − 0.9pF
$q_{\max}$	2.3pC
$\overline{i^2_{M,\text{d}}}/\Delta f$	$117.7\text{pA}^2/\text{Hz}$
$\overline{i^2_{RL}}/\Delta f$	$99.2\text{pA}^2/\text{Hz}$
$\overline{i^2_{CV}}/\Delta f$	$7.9\text{pA}^2/\text{Hz}$

Table 2: Oscillator design for example 1.

Constraint	Specification	Achieved
Phase Noise 600kHz	minimize	-118.5dBc/Hz
ω_{res}	1.8GHz	1.8GHz
C_{load}	$\geq$ 0.2nF	0.2nF
I_{tail}	$\leq$ 1.6mA	1.6mA
V_{sw}	$\geq$ 2V	2V
Tuning range	$\geq 10\%$	10%
d_{out}	$\leq 300\mu$m	300μm
Excess loop gain α_g	≥ 3	3

Table 3: Specifications for example 2.

Inductor	
L	10.0nH
n	6
d_{out}	300μm
w	13.0μm
s	1.8μm
R_s	17.4Ω
C_L	0.24pF
$R_{L,p}$	804Ω
Varactor	
$C_{\text{v,max}}$	0.32pF
$C_{\text{v,min}}$	0.16pF
$R_{v,p}$	$10.7\text{k}\Omega$

Transistors	
W_n/L_n	$6.8/0.35\mu$m
W_p/L_p	$21.0/0.35\mu$m
C_{NMOS}	0.03pF
C_{PMOS}	0.08pF
g_{m}	2.4mS
$1/g_{\text{ds,n}}$	$15.8\text{k}\Omega$
$1/g_{\text{ds,p}}$	$5.0\text{k}\Omega$
Tank	
R_{tank}	1250Ω
C_{tank}	0.43pF − 0.36pF
$q_{\max}$	0.71pC
$\overline{i^2_{M,\text{d}}}/\Delta f$	$38.0\text{pA}^2/\text{Hz}$
$\overline{i^2_{RL}}/\Delta f$	$41.0\text{pA}^2/\text{Hz}$
$\overline{i^2_{CV}}/\Delta f$	$3.1\text{pA}^2/\text{Hz}$

Table 4: Oscillator design for example 2.

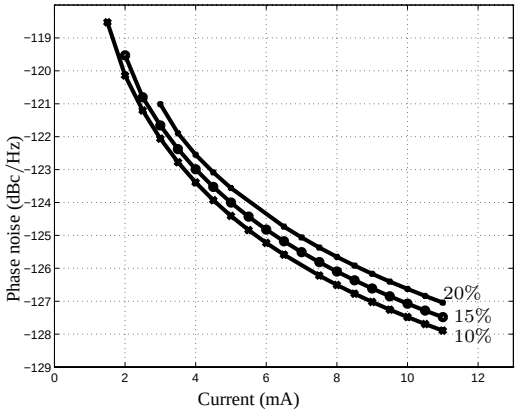

Figure 5: Minimum phase noise versus power limit for different tuning ranges.

7 Trade-off curves

By repeatedly solving optimal design problems as we sweep over values of some of the specifications, we can obtain globally optimal trade-off curves for the LC oscillator. In Figure 5 we show the trade-off curves of the minimum achievable phase noise versus quiescent power for different three tuning ranges. The rest of the specs are set to the values in table 2. As an RF designer might suspect, the phase noise decreases with higher power and smaller tuning range. What is difficult to know, without using the tool described in this paper, is exactly how these parameters trade off.

8 Conclusions

In this paper, we have shown how a commonly used LC oscillator can be optimized *rapidly* and *globally* by posing the design problem as a geometric program. This formulation permits the designer to quickly explore globally optimal tradeoff curves between different specifications. The method allows the simultaneous optimization of all passive and active components.

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