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QCN Implementation on Hardware

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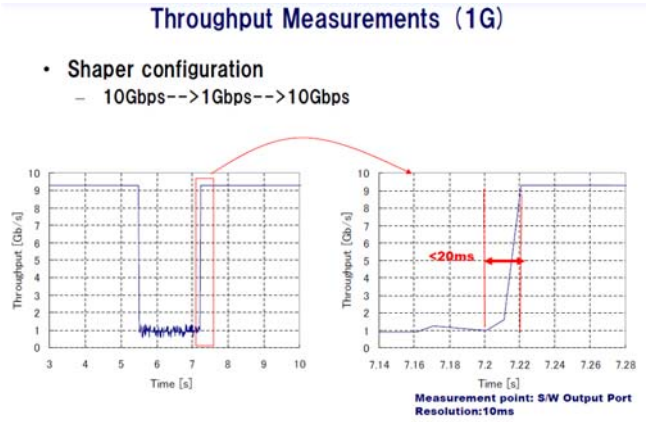
Overview

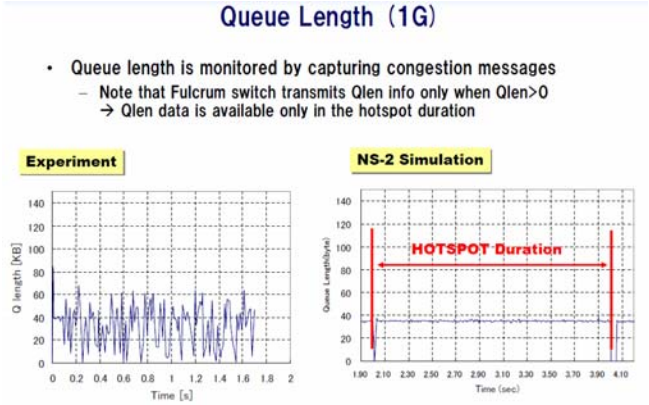
- World's first Hardware QCN Full implementation
  - It is fully functional
  - We confirmed that the result matches NS-2/OMNet simulation result!
    - We'll show in the next presentation by Abdul
- Features
  - QCN-NIC
    - Multiple Reaction Points
    - Improved Token Bucket Rate Limiter
  - QCN-Switch
    - Multiple Congestion Points
  - Compliant with Pseudo Code v2.3 [1]
  - 1Gpbs Platform

[1] QCN Pseudo Code v2.3: http://www.ieee802.org/1/files/public/docs2009/au-rong-qcn-serial-hai-v23.pdf

Background

- Previous implementation
  - We have presented QCN-NIC First implementation at IEEE Meeting in Jan 2009 (New Orleans)
  - We succeeded in basic QCN rate control





- Updates from previous implementation
  - Improved Rate Limiter function on QCN-NIC
  - Fully Implemented QCN Switch
  - Fully Implemented Multi-Source QCN Function
  - Various kinds of flexibility (Parameter , Modularity, Topology, etc..)

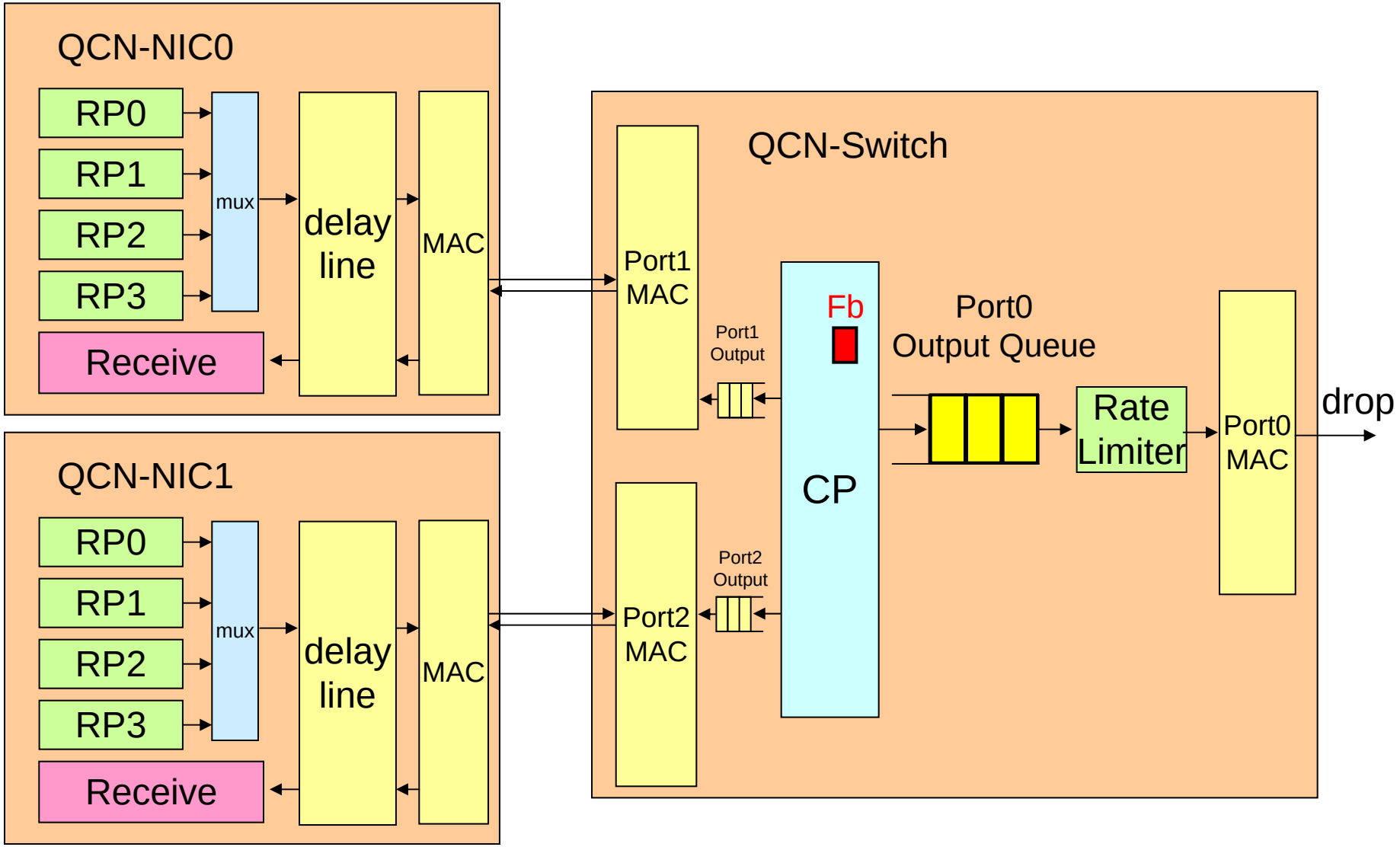
Our Implementation

Implementation on actual hardware

- FPGA Board
  - Implementation platform is NetFPGA [2]
  - FPGA: Xilinx Virtex-II Pro 50
    - Frequency: 125MHz
    - Internal data bit width: 64bits -> 8Gbps
  - 4MB SRAM
  - 1Gbps Ports x 4

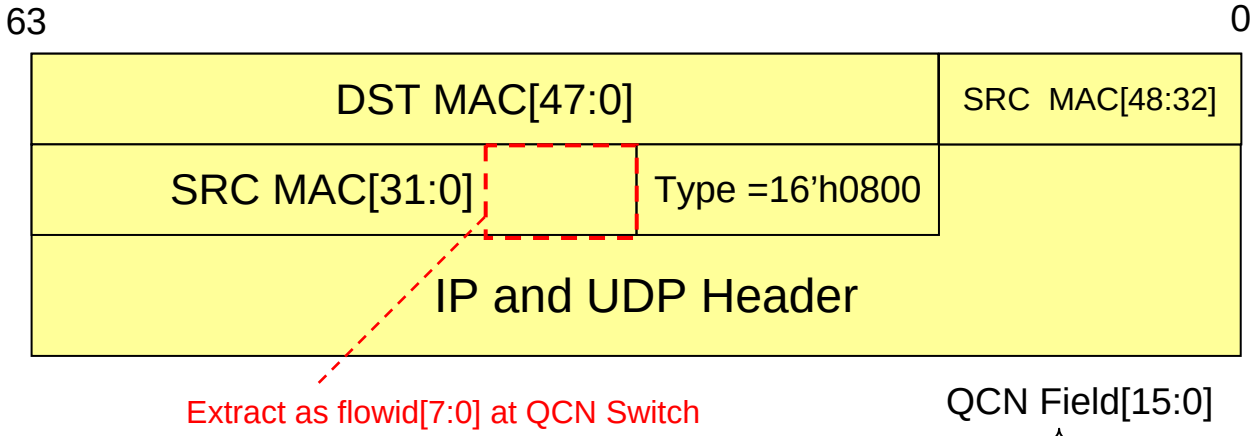
[2] NetFPGA Project : http://www.netfpga.org

System Level Architecture

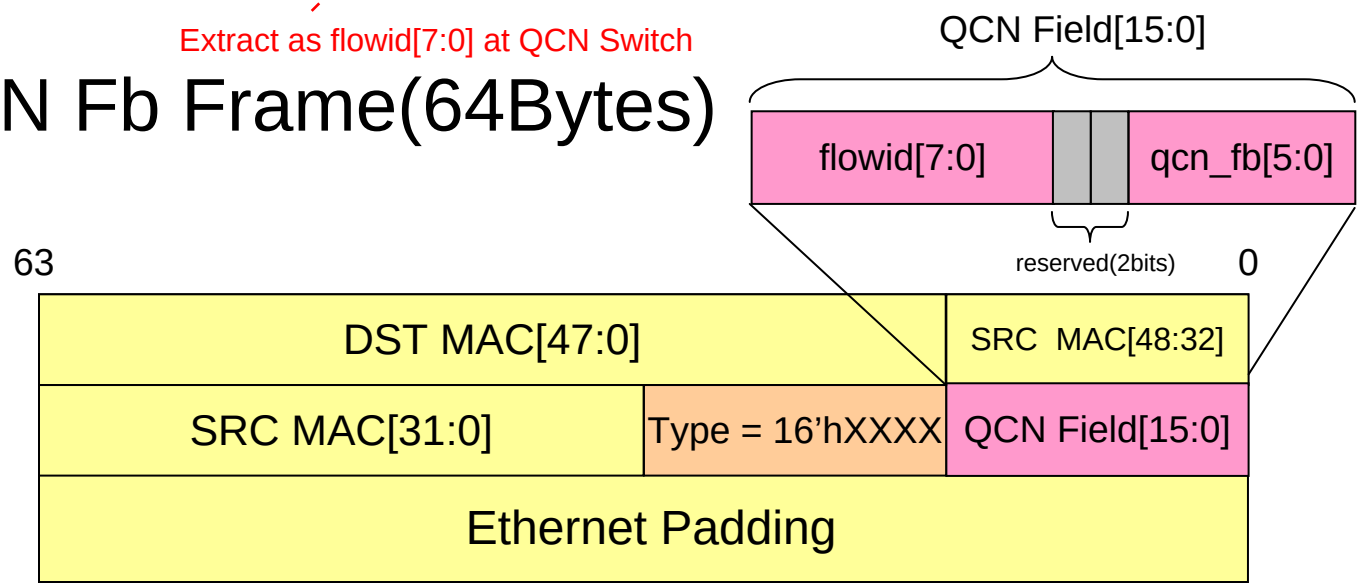


Packet Format (temporal)

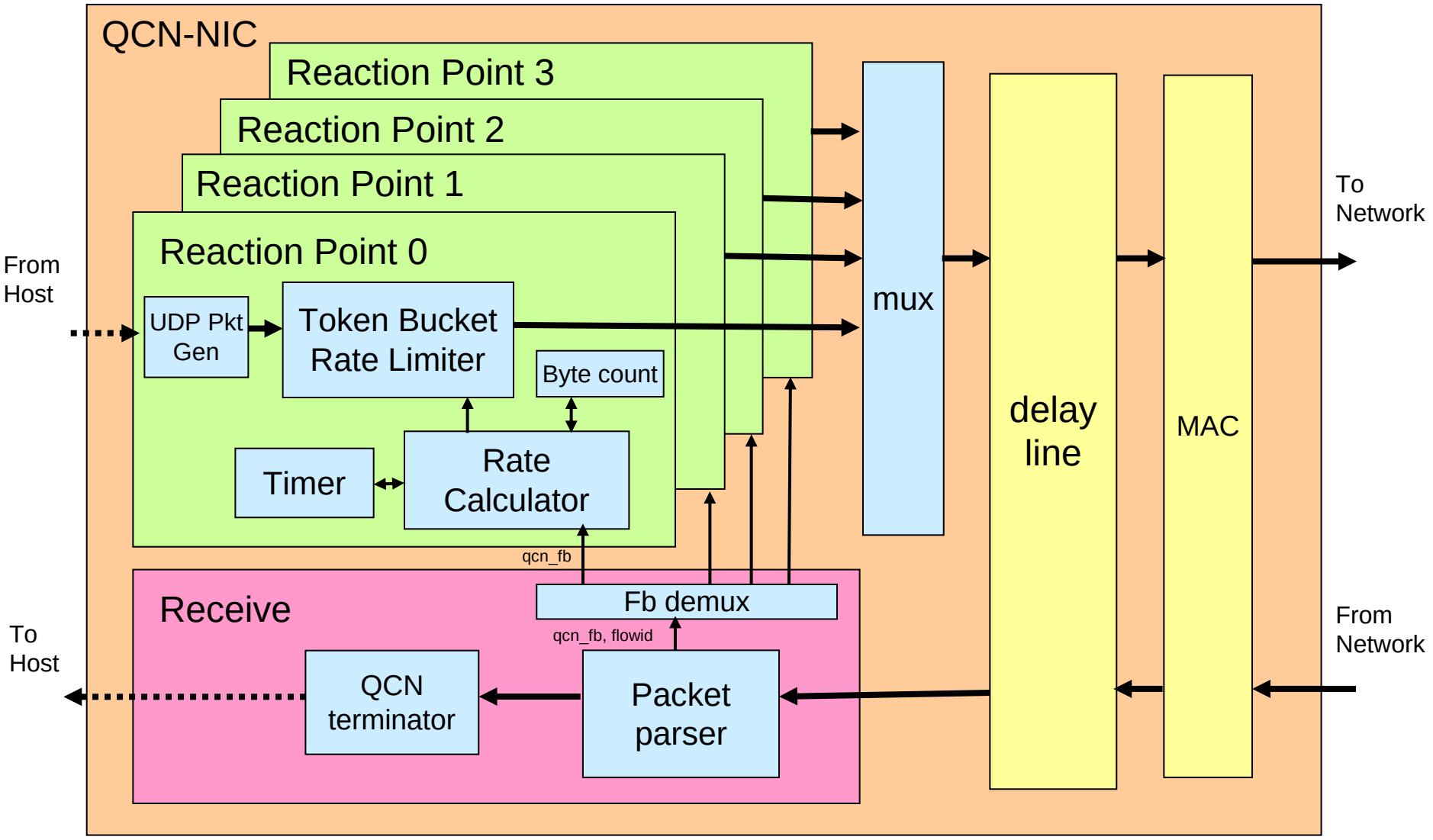
- Data Frame (Normal Ethernet UDP/IP Frame)



- QCN Fb Frame(64Bytes)

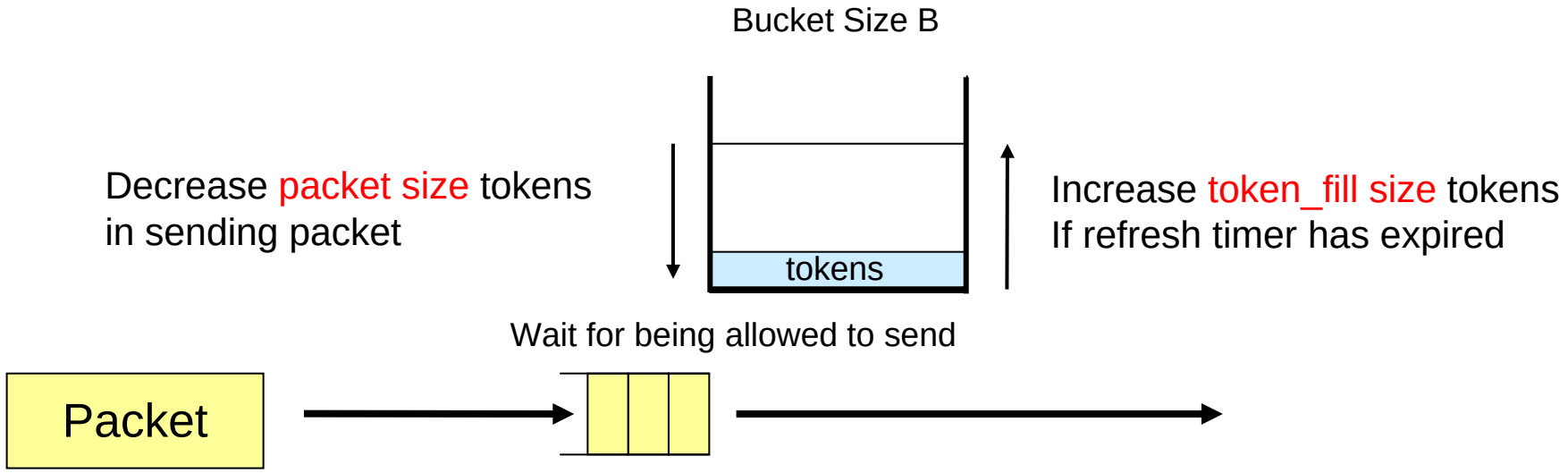


QCN NIC Architecture



Improved Token Bucket Rate Limiter

- We improved the token bucket algorithm to avoid burstiness



Previous implementation

Send Condition:
tokens in the bucket > 0

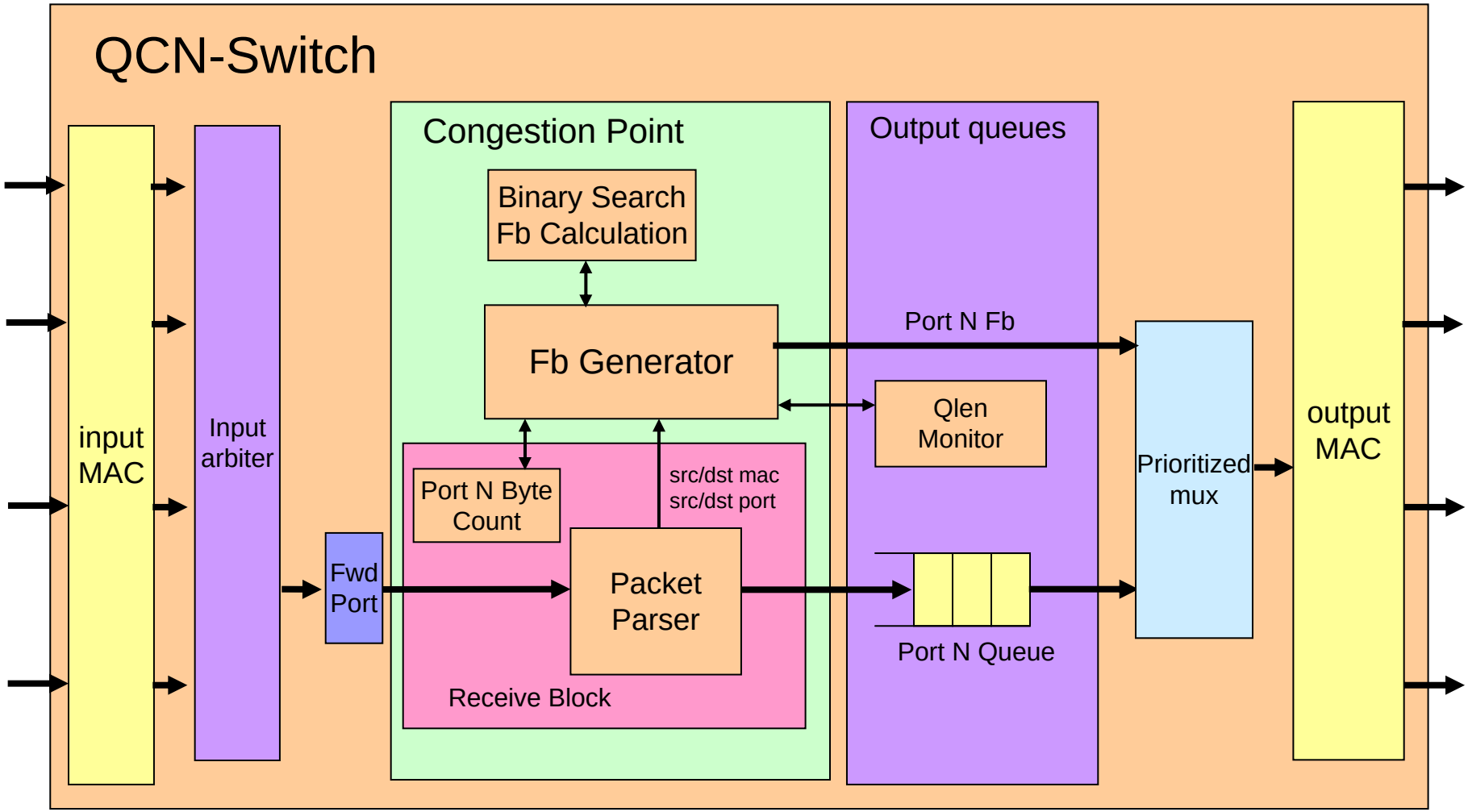
Causing burstiness!

Current implementation

Send Condition:
tokens in the bucket >= token size

Working Fine

QCN Switch Architecture



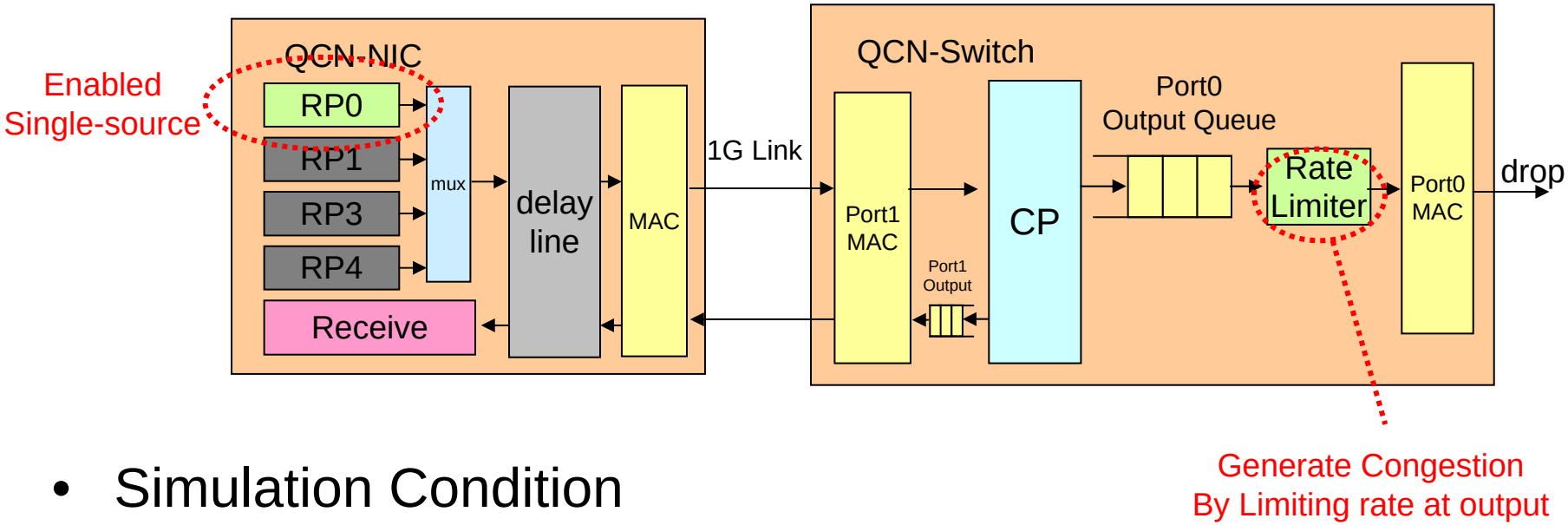
(N: Number from 0 to 3)

Supported QCN Functions

- QCN NIC
  - ☑ Fast Recovery
  - ☑ Extra Fast Recovery
  - ☑ Active Increase
  - ☑ Hyper Active Increase
  - ☑ Target Rate Reduction
  - ☑ Byte Counter Jitter
  - ☑ Timer Counter Jitter
  - ☑ 150K/75K Byte Counter stretching
  - ☑ Timer Counter stretching
- QCN Switch
  - ☑ Byte Counter Jitter
  - ☑ Adjustable sample time (lookup table)

QCN Test: RTL Simulation

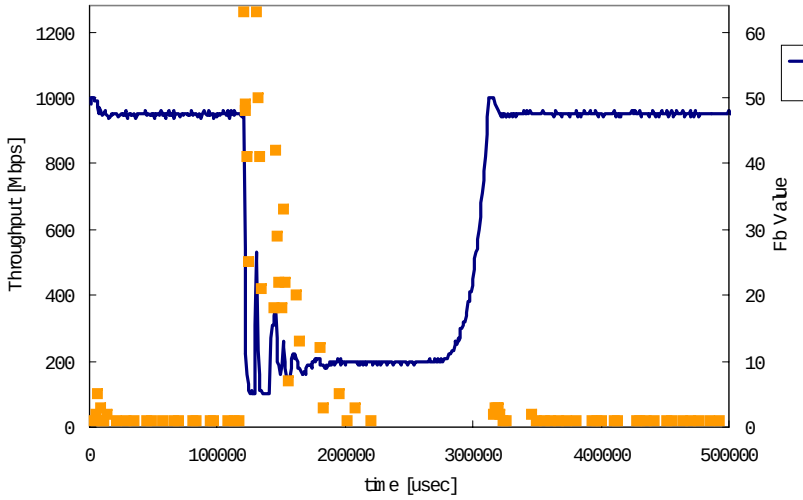
- RTL Simulation System



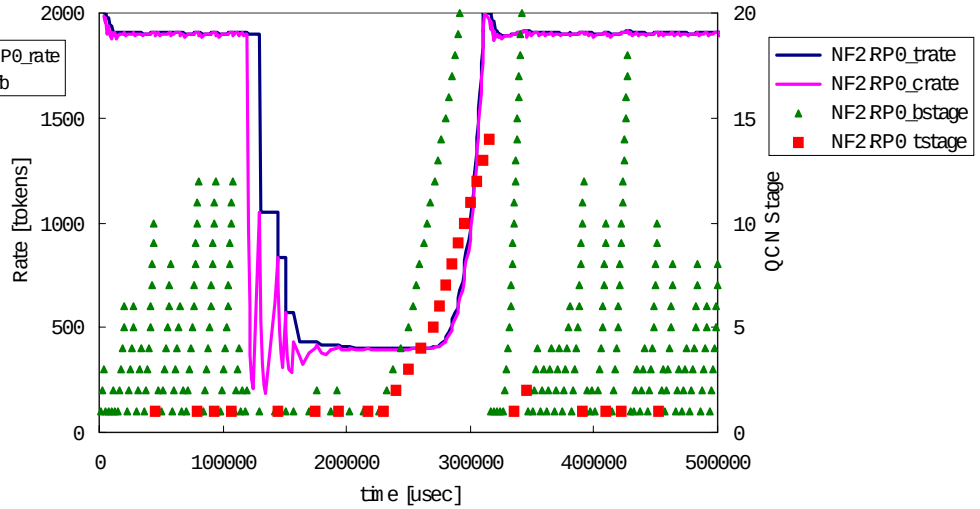
- Simulation Condition
  - Reaction Points: 1 (Single-Source)
  - Delay Disabled
  - Rate Limit: 950Mbps -> 200Mbps -> 950Mbps
  - Detailed parameters are shown in the next session.

QCN RTL Simulation Result

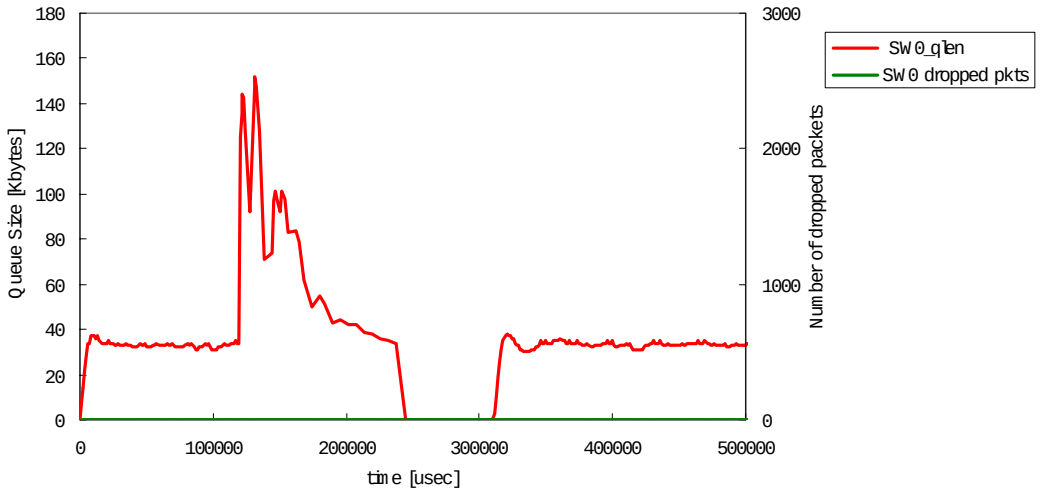
Throughput & Received Fb value



QCN NIC Parameters



Switch Queue Length & Packet Drop



Conclusion

- We’ve developed QCN full implementation
- All QCN Functions are implemented (Pseudo Code v2.3)
- QCN-NIC
  - Multiple RPs are ready
  - Improved Token Bucket Rate Limiter
- QCN-Switch
  - Multiple CPs are ready
- We implemented on the NetFPGA Board (1Gbps system)
- Logic is portable (not platform dependent) and simple
  - We can easily migrate to 10G platforms

- The detailed hardware evaluation results will be shown in the next session.